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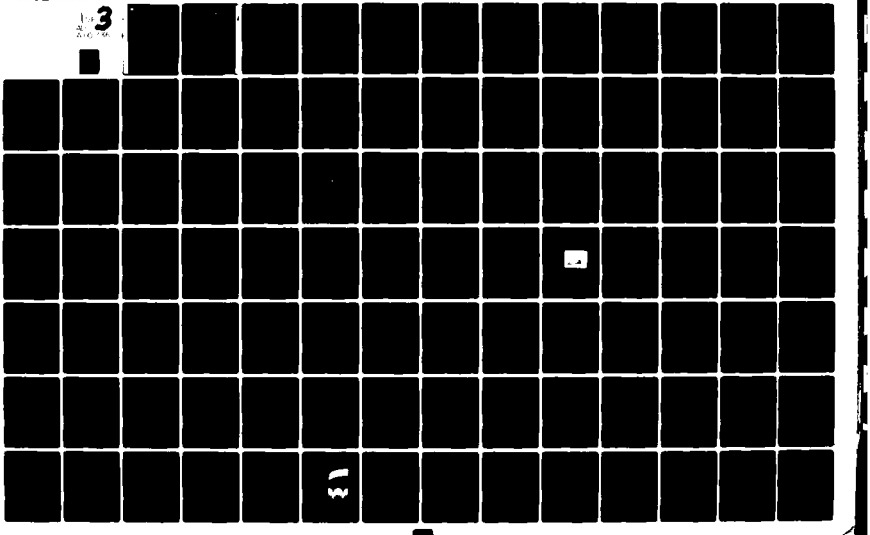

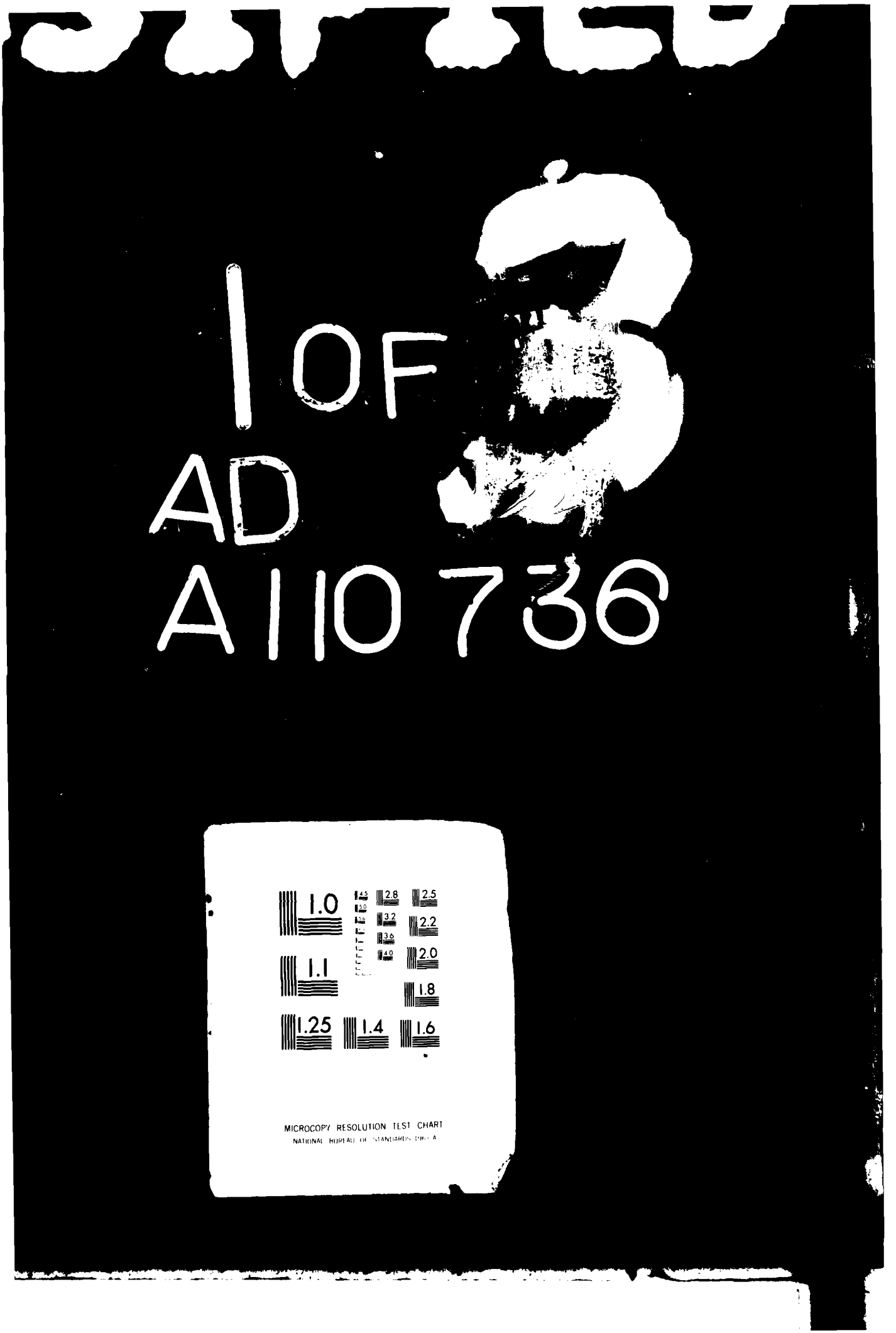
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PERFORMANCE LIMITS ON GaAs FET LARGE- AND SMALL-SIGNAL CIRCUITS

D. R. GREEN, JR.
F. J. ROSENBAUM

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October 1981

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A describing function approach to large-signal frequency-domain simulations of nonlinear microwave circuits is presented. It is used to examine gain saturation and harmonic distortion of a 0.5 μm gate FET. The simulation uses a previously reported FET model, modified to include gate breakdown and substrate leakage current. Temperature effects are studied. It is found that gain saturation does not depend on gate breakdown. The model is verified by comparing theoretical and experimental performance.

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Performance Limits on GaAs FET Large- and Small-Signal Circuits

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NONLINEAR MICROWAVE MESFET MODELING

FOR

LARGE-SIGNAL CIRCUIT DESIGN

1. INTRODUCTION

Compound semiconductor, especially gallium arsenide, metal-semiconductor field effect transistors (MESFETs) are increasingly being used for large-signal microwave applications such as power amplifiers (1,2)*, oscillators (3), mixers (4), frequency multipliers (5), and logic circuits (6). The principles of field effect transistor (FET)

*The numbers in parentheses in the text indicate references in the bibliography.

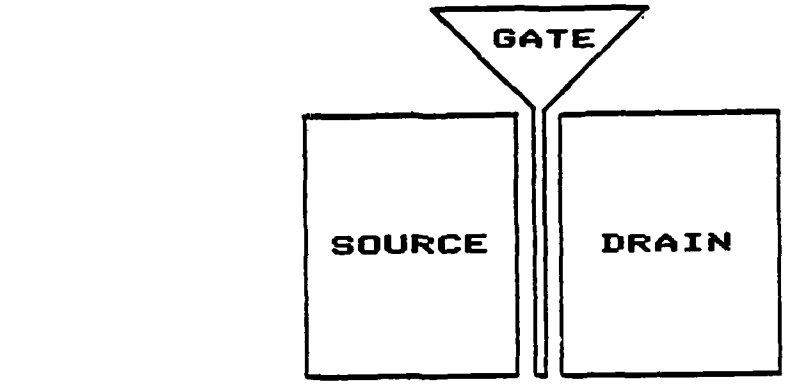
operation are reasonably well understood: small-signal transistors have been modeled (7), and linear circuits have been designed using conventional techniques. However, due to the complications presented by nonlinear MESFET behavior under large-signal conditions and the resulting nonlinear interaction of the transistor with its external circuit, it is difficult at present to confidently design or conveniently predict the large-signal performance of MESFET circuits. Consequently, large-signal MESFET circuit design tends to be empirical. However, prototype circuit construction can be costly - especially for monolithic microwave integrated circuits. This motivates the development of nonlinear microwave MESFET models that can be effectively used for large-signal circuit design. Likewise, compatible large-signal circuit design techniques are of concurrent interest and importance.

The purpose of the work presented here is to improve MESFET modeling techniques, and investigate large-signal circuit simulation methods in order to verify the effectiveness of the modeling and improve computational efficiency in obtaining steady-state results.

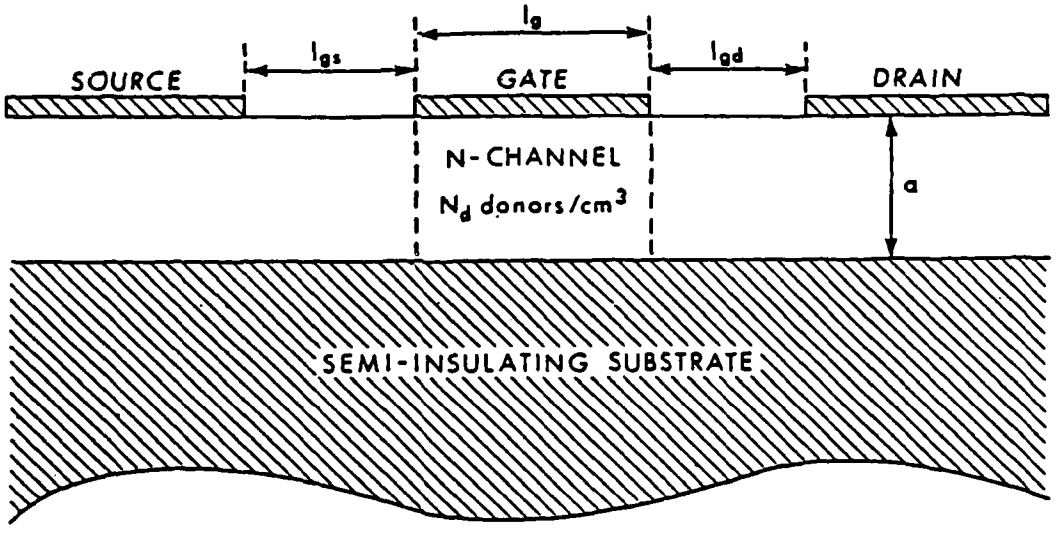
1.1 MESFET STRUCTURE

Microwave MESFETs (8) may be realized in planar form as shown, for example, in top view and cross section in Figure 1.1. Devices are fabricated on n-type GaAs located on a semi-insulating GaAs substrate. Source and drain metallizations provide ohmic contacts for the channel. The gate metallization forms a Schottky barrier (9). In operation, the drain-source voltage is positive. Electrons flow from the source contact, through the n-type layer, under the gate, and to the drain contact. For depletion mode operation, the gate-source voltage is negative, and a depletion region exists under the gate which narrows the channel through which the electrons flow. Larger negative gate-source voltages further extend the depletion region and increase the drain-source resistance. In this manner, the gate-source voltage controls the source-drain current.

Gate length is denoted by l_G in the Figure 1.1. Gate-source and gate-drain spacings are l_{GS} and l_{GD}, respectively. The gate width is the dimension of the gate in the direction into the plane of the illustration. For a microwave MESFET ,the gate length is of the order of one micron, and the gate width may be several hundred microns. The n-type layer height is denoted by a. For GaAs MESFETs, the n-type layer can be created by epitaxial



TOP VIEW



CROSS-SECTION

Figure 1.1 Top and cross section views of a simple MESFET.

growth on a semi-insulating (compensated) GaAs substrate, or directly by ion implantation.

The gate length is made as short as possible to reduce the electron transit time under the gate, where most of the current control occurs, to thereby achieve high frequencies of operation. For this reason also, compound semiconductors such as GaAs are preferred over Si because of their greater electron mobilities. The power handling capabilities of the MESFET scale upward with the gate width, because this increases the current that the device can handle. In practice, several source-gate-drain combinations are connected in a parallel interdigitated fashion in order to eliminate traveling voltage wave effects which can occur along extended single gate structures. This interconnection is referred to as a cell. To further increase power, multiple cells can be connected in parallel. A top view of a commercial MESFET used in experiments to be reported later in this dissertation is presented in Figure 1.2.

1.2 MESFET MODELING STRATEGIES

There are two approaches to nonlinear MESFET modeling, although some strategies combine elements of both: "black box" and physical. In either case, it is desirable for the model to be lumped, rather than

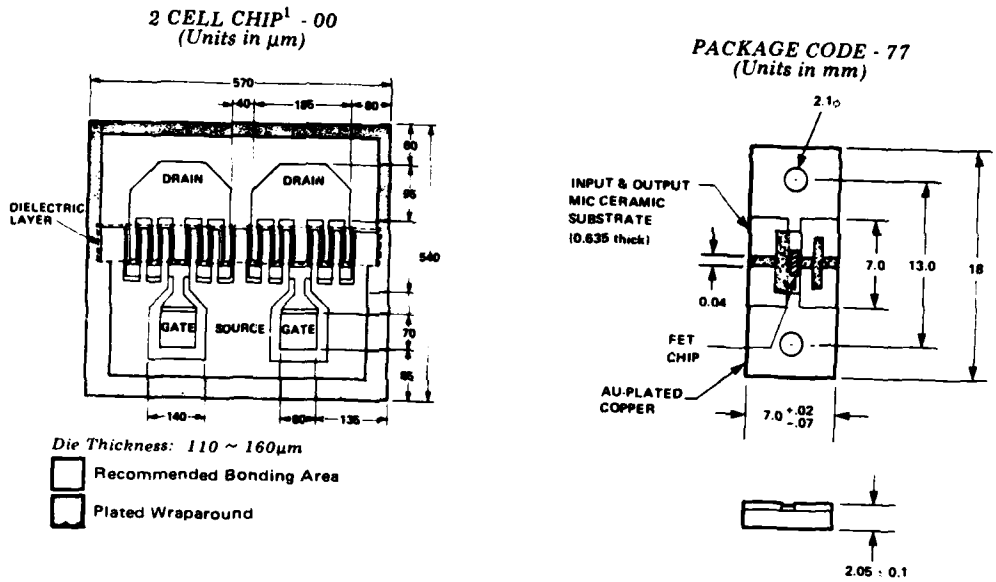


Figure 1.2 Top view of a NEC NE869177-10 K-band MESFET. (Courtesy of the Nippon Electric Company.)

distributed, in order to facilitate large-signal circuit simulation. For present purposes, this is equivalent to the requirement that the model's output variables be uniquely determined by the instantaneous values of the input variables and their first order time derivatives.

A recent example of a hybrid "black box"-physical approach is the large-signal GaAs MESFET model reported by Tajima et. al. (10). This model combines empirical drain current characteristics with approximate theoretical expressions for some of the nonlinear capacitances associated with the transistor.

1.2.1 "Black Box" Modeling Approaches

The "black box" approach relies on a set of measurements that is devised to characterize the transistor in such a way that its general nonlinear behavior can be predicted. This is exemplified by the work of Willing, Rauscher and de Santis (11), which assumes a physically motivated MESFET equivalent circuit, and determines the behavior of the voltage controlled nonlinear elements on the basis of numerous small-signal S-parameter measurements of specific transistors over a range of bias voltages.

The drawbacks of such an approach are: first, that extensive small-signal measurements must be made for each

new type of MESFET to be characterized; and second, the assumption that such small-signal, incremental, measurements - even though taken over an extensive range of D.C. bias voltages - provide suitable information for predicting large-signal behavior. An obvious limitation of this assumption is that practically, the MESFET operates over a range of temperatures corresponding to the power dissipation at different bias voltages for the set of small-signal measurements; whereas in large-signal microwave operation, the MESFET operates isothermally at a temperature corresponding to the average power dissipation over a microwave period. This will be discussed further in Section 2.1.2.

There are alternative "black box" characterization techniques which are based on large-signal measurements. Examples include load-pull techniques (12) in which measurements are taken under large-signal conditions as the fundamental frequency terminating impedances presented to the transistor are varied. Unfortunately, it is very difficult to control the impedances loading the transistor at the harmonic frequencies present under large-signal conditions. This limits the usefulness of this technique when the MESFET is driven into grossly nonlinear behavior. Another large-signal characterization approach has been reported by Howes and Jeremy for solid state devices in microwave oscillator applications (13). It involves the

construction of circuits which are similar to the intended application, and the systematic variation of circuit parameters while measuring performance. Although this is an orderly way to proceed and may provide useful design insight, it is also almost an empirical prototype construction approach, with the attendant potentially high costs.

1.2.2 Physical MESFET Modeling Approaches

Physical models are derived mathematically from the semiconductor physics underlying FET behavior. With simplifying assumptions, models such as Shockley's original analysis (14) can be derived analytically. Unfortunately, the simplifying assumptions that make an analytic treatment possible result in models that are inadequate for predicting microwave MESFET performance. For example, electron velocity saturation and two-dimensional field effects are often neglected. Attempts to improve the Shockley model (15-18), mainly by including velocity saturation effects, are of limited usefulness in small-signal applications. Curtice (19) has recently presented a large-signal MESFET model, developed along similar lines, specifically for use with a commercially available computer aided circuit design software package.

Computer simulations involving the two-dimensional numerical solution of the partial differential equations describing charge transport in the FET (20-25) have proved helpful in the detailed understanding of the physical processes dominating the device's behavior. However, very long computation times are encountered which render such classical numerical approaches prohibitively expensive for large-signal circuit design.

Fortunately, among the reported numerical simulations, Yamaguchi and Kodera (26) have performed an extensive enough investigation to permit their formulation of a parametric expression for carrier density in the active region of the MESFET under the gate. This model will be described in more detail in Section 1.3. Additional large-signal MESFET models based on this formulation have since been reported. Shur and Eastman (27) have directly used the Yamaguchi-Kodera model in conjunction with a representation they developed to model charge accumulation effects. This modification is questionable and will be examined in detail in section 2.1.3. Shur and Eastman use their implementation to calculate static drain current characteristics and small-signal capacitances. Madjar and Rosenbaum have developed a large-signal MESFET model which is also based on the Yamaguchi-Kodera results. This work (28,29)

provides the basis for the modeling which follows in this report and will be described in Section 1.4.

MESFET modeling which is based upon numerical simulation results is promising because it is potentially capable of describing devices that have not yet been fabricated, and providing information about the optimization of fabrication parameters for specific applications. The approximations made in the direct derivation of analytic models generally would be expected to render them unsuitable for this purpose.

1.3 THE YAMAGUCHI AND KODERA FET MODEL

The FET model which serves as the foundation for the MESFET modeling presented here was published by Yamaguchi and Kodera (26) in 1976. It is based upon a physical picture resulting from numerous two-dimensional numerical solutions of the partial differential equations describing charge transport in the transistor. Armed with this information, they formulated a simplified model for the carrier density under the gate as an implicit function of the internal gate-source and drain-source voltages. These voltages refer to the potentials at the dashed boundaries under the gate edges in Figure 1.1, and do not include the additional voltage drops between these boundaries and the actual source and drain contacts, which will later be

modeled as linear parasitic resistances. The region of the n-type layer under the gate is referred to as the "active region". This corresponding model will hereafter be referred to as the "basic FET model", which embodies all of the nonlinear aspects of the transistor's behavior.

The modeling of the charge distribution under the gate as an implicit function of the two controlling voltages obviates the need for further time consuming two-dimensional numerical solutions of the semiconductor equations. However, because the charge distribution is implicit, it must still be obtained iteratively. This involves equating the total conduction currents at the internal source and drain boundaries, which requires some one-dimensional numerical integration. The strategy used in the Madjar-Rosenbaum model to further reduce this computation time will be discussed in Section 1.4.

Once the charge distribution has been determined for the assigned internal drain-source and gate-source voltages, the drain conduction current is also known. The static depletion region charge and drain conduction current characteristics for the basic FET model are calculated in this manner. Additionally, Yamaguchi and Kodera calculate g_D, the derivative of the drain current with respect to the internal drain-source voltage, and g_M, the derivative of the drain current with respect to the internal gate-source voltage. They also calculate the

common-source incremental gate input capacitance from the depletion region charge characteristics.

It is worthwile to examine the assumptions made by Yamaguchi and Kodera in developing their model, in order to keep in mind inherent limitations and their implications for large-signal microwave circuit applications. These limitations are also present in the basic Madjar-Rosenbaum MESFET model, since it is based on the work of Yamaguchi and Kodera. The assumptions and their implications are:

1.) Uniform channel doping: This limits the usefulness of the model for MESFETs fabricated with nonuniform doping.

2.) Monotonic electron velocity-electric field relationship: GaAs exhibits negative differential mobility which can lead to Gunn instabilities (30) and charge accumulation effects not included in the model. This will be discussed further in Section 2.1.3.

3.) There is no gate conduction current in the Yamaguchi-Kodera simulations : Gate conduction current may significantly affect large-signal MESFET performance. This issue will be addressed in Sections 2.3.1 and 5.2.

4.) Substrate current was not present in the Yamaguchi- Kodera simulations : In some presently

available microwave MESFETs substrate current represents a non-negligible parasitic effect. Correction of the basic model, as necessary, will be discussed in Section 2.1.4.

5.) Resistances and reactances arising from regions of the MESFET outside the "active region" are considered to be linear, and are not included in the basic model: A method for calculating the parasitic resistances will be presented in Section 2.1.1. Parasitic reactances will be calculated from small-signal measurements of a MESFET in Section 2.2.

1.4 THE MADJAR-ROSENBAUM LARGE-SIGNAL MESFET MODEL

The Madjar-Rosenbaum MESFET model (28,29) is based upon the Yamaguchi-Kodera FET model described in the previous section. Computation time was substantially reduced by introducing a predictor-corrector algorithm to determine the charge distribution under the gate. Creation of the predictor involved the derivation of analytic approximations for the source and drain conduction current integrals to permit the explicit calculation of the drain current and associated MESFET parameters as functions of the internal gate-source and drain-source voltages, hereafter referred to as V_1 and V_2, respectively.

This was a formidable task, resulting in nine different sets of equations corresponding to charge distribution and electric field conditions in the MESFET. These are detailed in Reference 28. The predictor was originally written for, and tested against experimental drain current characteristics for a 1.7 micron gate length MESFET, requiring one corrective iteration at most. This author has successfully used the algorithm with gate lengths as short as 0.5 micron, with a maximum of three corrective iterations. The requirement for rapid convergence is that the gate length to active layer height aspect ratio be greater than two.

The input data required by the model is: gate length, gate width, active layer height, built-in potential of the Schottky barrier, relative dielectric constant, saturated electron velocity and critical field. In addition to the drain conduction current, the Madjar-Rosenbaum model also calculates g_M, g_D, electron transit time, and R_C, an effective gate series charging resistance. An incremental capacitance matrix is also available to calculate gate and drain displacement currents from the first order time derivatives of V_1 and V_2. The equivalent circuit is illustrated in Figure 1.3. The current-voltage relationships for the three terminal, nonlinear, nonreciprocal capacitance are shown in Figure

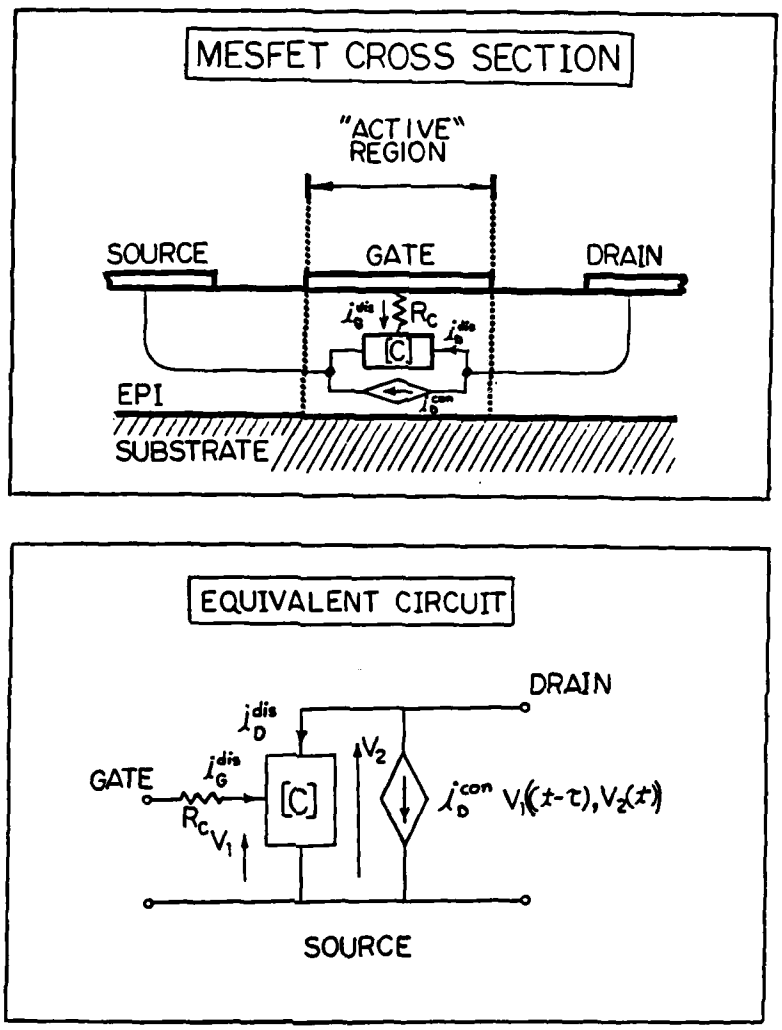


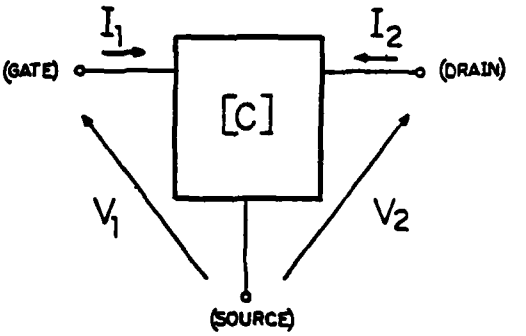
Figure 1.3 Equivalent circuit for the Madjar-Rosenbaum basic MESFET model.

1.4. Although such a three-terminal element may appear unfamiliar, it is a valid and useful concept in this context. The nonlinear circuit theory relevance of multiterminal elements, in general, is discussed in Chapter 2 of Stern (31).

The functional forms of typical output from the model are illustrated in Figures 1.5 and 1.6. Electron transit time is essentially constant for values of V2 greater than 100 millivolts. These five surfaces contain all of the information required from the basic nonlinear MESFET model for large-signal circuit simulation and design using a particular transistor. A method that exploits this observation to greatly reduce the computation time for numerical large-signal circuit simulation wil be introduced in Section 3.2.

1.5 LARGE-SIGNAL CIRCUIT ANALYSIS AND DESIGN STRATEGIES

The most obvious steady-state dynamic nonlinear circuit analysis method is numerical time-domain integration. State variable differential equations are derived for the circuit, and initial guesses are assigned to the state variables. This results in an initial value problem. Numerical integration (32) then proceeds until steady-state is achieved; that is, all of the state variables assume the same values at the beginning and end



$$\begin{bmatrix} i_G^{dis} \\ i_D^{dis} \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

WHERE: $C_{ij} = C_{ij}(V_1, V_2)$
$i, j = 1, 2$

Figure 1.4 Terminal current-voltages for the nonlinear, nonreciprocal three terminal capacitance of Figure 1.3.

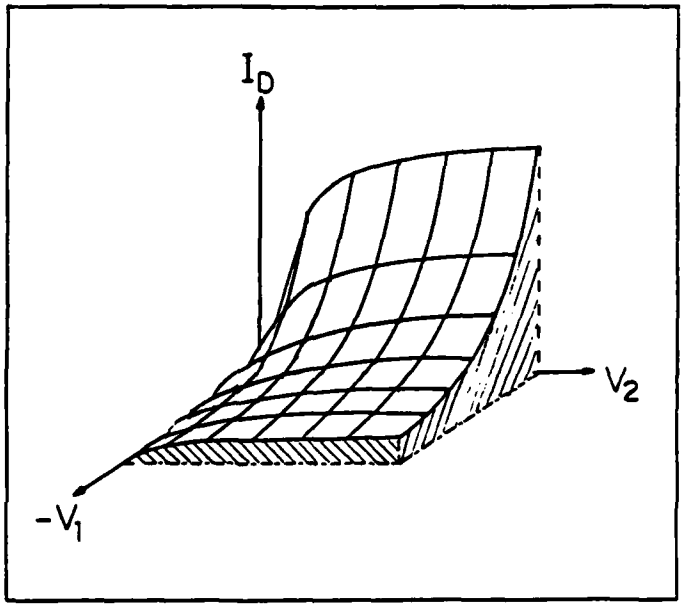


Figure 1.5 Stylized form of drain current output from the Madjar-Rosenbaum basic MESFET model, as a function of V_1 and V_2, the internal gate-source and drain-source voltages.

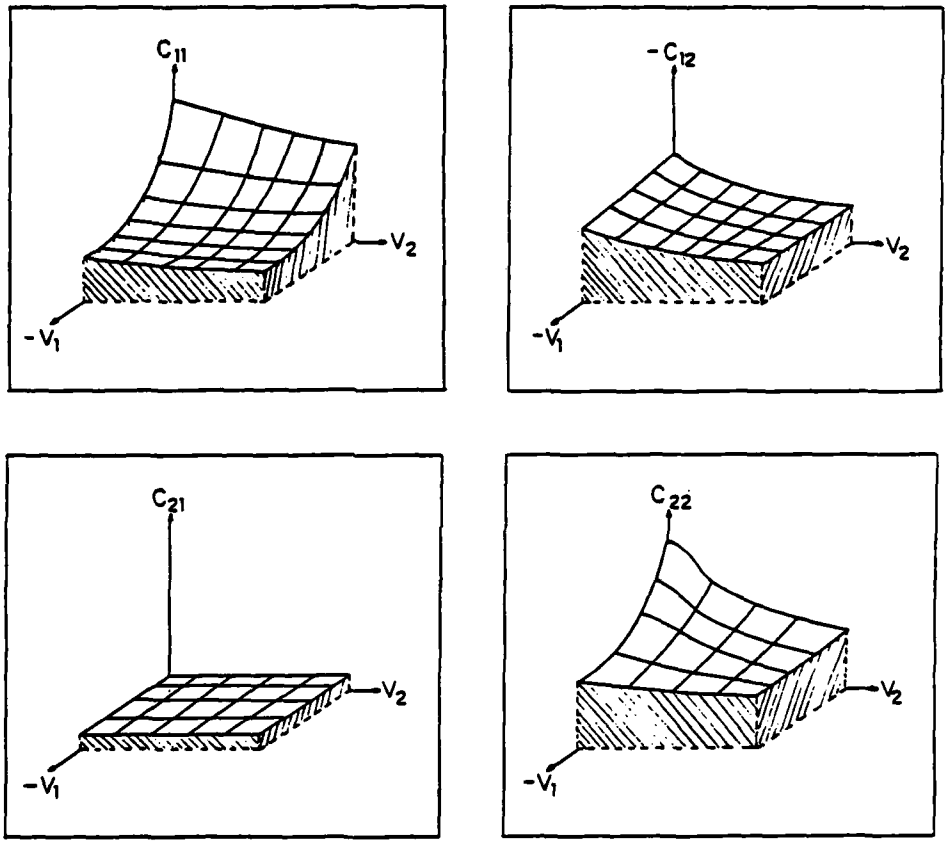


Figure 1.6 Stylized forms of the incremental capacitance matrix entries modelling displacement currents in the Madjar-Rosenbaum basic MESFET model.

of a period. A major drawback of this method is that integration over many periods may be required if the initial guess for the steady-state values of the state variables is too far off, or if time constants associated with the circuit differ by orders of magnitude. "Shooting methods", which are a two-point boundary value problem approach have been proposed to reduce the computation time required to reach steady-state (33).

Other disadvantages are that the number of state variables increases with the number of reactive elements in the circuit, and distributed elements can only be approximated with networks composed of lumped elements. Allen (34) has proposed a scheme to overcome these disadvantages. Superposition for the linear parts of the circuit is utilized in a convolutional representation which is calculated at each integration step.

Harmonic balance frequency-domain simulation approaches (35) have been devised which also make use of superposition for the linear subnetworks of the circuit. The measured or calculated frequency response of the linear parts of the circuit is used, and the variables to be determined are the phasor voltages and currents (fundamental and harmonic) at the linear network-nonlinear network interface as illustrated in Figure 1.7. The solution is obtained using a nonlinear optimization algorithm (36) to match the currents and voltages at the

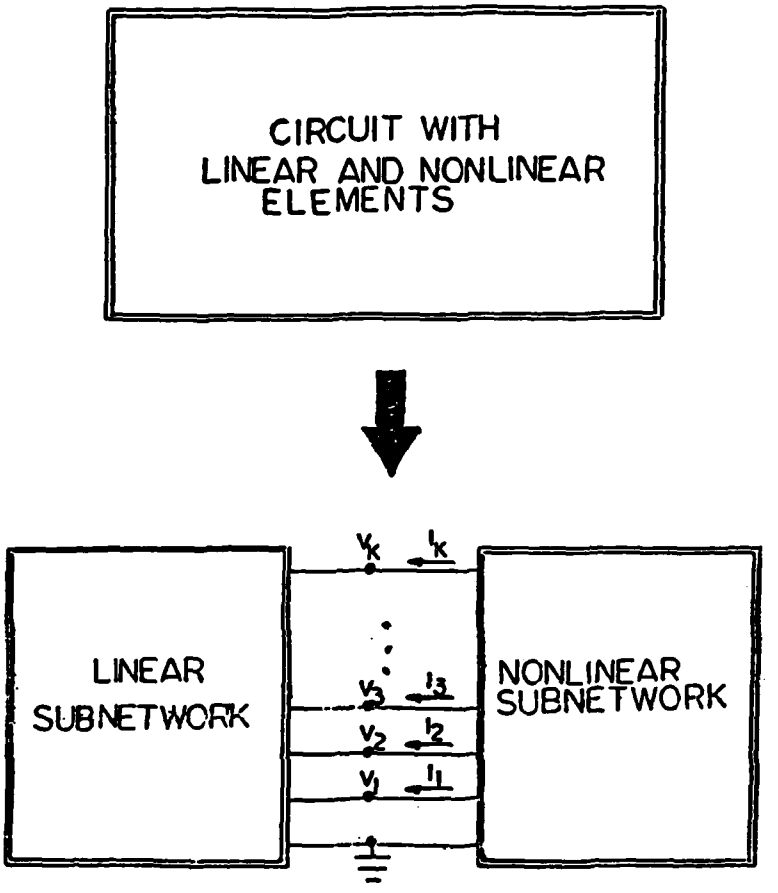


Figure 1.7 Division of a circuit containing linear and nonlinear elements, into subnetworks consisting of linear or nonlinear elements exclusively.

interface. Only the response of the nonlinear subnetwork needs to be calculated in the time-domain.

A fundamental limitation common to all of the circuit simulation techniques that are discussed above is that they only indicate how a particular circuit performs under a specified set of conditions. Attempts to optimize circuit performance and gain design insight invariably require numerous circuit simulations. It is possible to use conventional frequency-domain circuit design techniques in large-signal design situations if the nonlinear MESFET model can be used to calculate a compatible large-signal frequency-domain representation of the transistor's terminal behavior. Such a representation is called a "describing function" and has found wide use in nonlinear control system design (37), but is a relative newcomer to dynamic nonlinear circuit design (38). Unfortunately, the use of such a describing function representation appears to be limited to two terminal nonlinear devices unless certain constraints are applied, or assumptions made. More will be said of this in conjunction with the design applications discussion in Chapter 6.

1.6 SCOPE OF THIS STUDY

The contributions of the work reported here are the modifications and extensions of the Madjar-Rosenbaum MESFET model in order to improve its applicability for large-signal circuit analysis and design, and the investigation and application of circuit analysis and design procedures that make the best use of such a model. Verification of the model as it evolves, involves comparison with experimental results. The sequence is shown in Figure 1.8. For a lumped model such as that derived here, a reasonable match between experimental and predicted results for each step is a necessary condition for success in the following step.

Chapter 2 starts with an investigation of static nonlinear current-voltage characteristic modeling, including temperature and charge accumulation effects. Modeling of small-signal S-parameters follows. A discussion of gate conduction current is begun, and the chapter concludes with a discussion of an upper frequency limit on the validity of the lumped model approximation.

Chapter 3 demonstrates the use of the model for conventional time-domain large-signal circuit simulations. The numerical integration algorithm is described, and a look-up table technique for using the MESFET model results is introduced to reduce computation time. A frequency

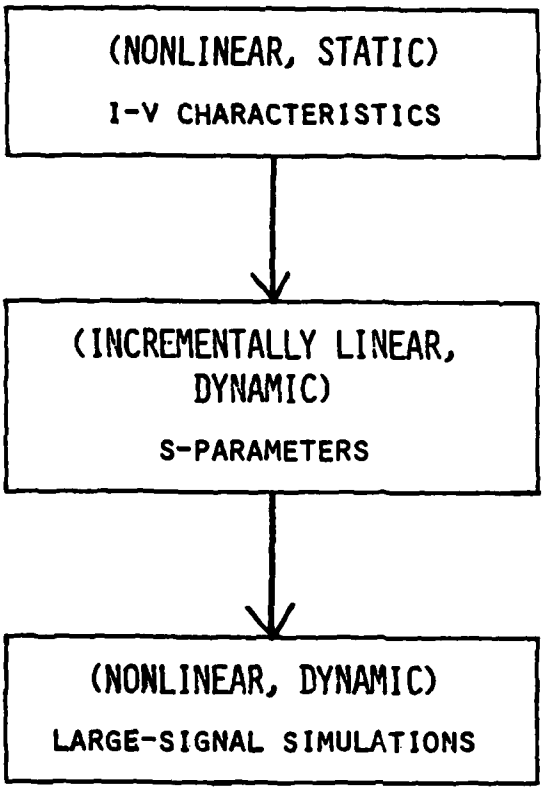


Figure 1.8 Verification sequence used in comparing measured results with results predicted by the MESFET model.

doubler circuit is simulated, and the results are compared with experimental results (performed elsewhere) using a similar MESFET.

Chapter 4 describes modifications to the model for the efficient calculation of frequency-domain currents from frequency-domain voltages. This is useful for frequency-domain large-signal nonlinear circuit simulation which is also introduced.

Chapter 5 presents experimental results for an overdriven MESFET amplifier, and corresponding simulation results obtained with the frequency-domain simulation algorithm of Chapter 4. The MESFET model is augmented with a gate conduction current model. Of particular interest is the large-signal role played by gate conduction current in gain saturation.

Chapter 6 reviews the large-signal MESFET model results, and compares the large-signal circuit design approaches that have been used with emphasis on potential utility in microwave circuit design. Additional applications are discussed.

2. MICROWAVE MESFET MODELING

This chapter describes the extensions that are used with the Madjar-Rosenbaum model , which was discussed in Section 1.4, in order to improve the correlation between experimental measurements and results calculated using the model. The sequence that was followed for this procedure is indicated in Figure 1.8.

The first step is the investigation of static current-voltage characteristics, which is covered in Section 2.1. This is used as the starting point because no reactances are involved.

The second step (incrementally linear, dynamic) is the calculation of small-signal scattering parameters that agree with measured scattering parameters. This involves the resistances and static nonlinearities of the first step, as well as linear parasitic reactances and incremental values of the nonlinear capacitances associated with the transistor. This is discussed in Section 2.2. Small-signal S-parameter match-up is also used to help determine values for some of the linear parasitic reactances, which are difficult to calculate *a priori*.

The third step is large-signal circuit simulation and comparison with experimental results. This depends

upon the parasitic elements, and the static nonlinearities examined in the first two steps, as well as nonlinear reactances. Preliminary considerations will be introduced in Section 2.3, and the discussion will continue in Chapters 3 and 5, which describe large-signal circuit simulations.

2.1 TERMINAL I-V CHARACTERISTIC CALCULATION

The basic MESFET model (Figure 1.3) does not include the source and drain contact resistances, or resistances associated with the voltage drops between the contacts and the "active region" of the MESFET. Consequently, static drain current characteristics such as are measured at the actual terminals of the transistor, must be calculated taking these resistances into account. Figure 2.1 is the circuit model used to calculate static I-V characteristics. A dependent drain current source is used to describe the nonlinear portion of the device. The dashed boundary contains this voltage controlled nonlinear current source. V_1 and V_2 are the internal gate-source and drain-source voltages used as inputs to the nonlinear model. V_G and V_D are the gate-source and drain-source voltages applied at the actual terminals of the transistor. R_S and R_D are linear parasitic resistances not included in the basic model. The problem is to

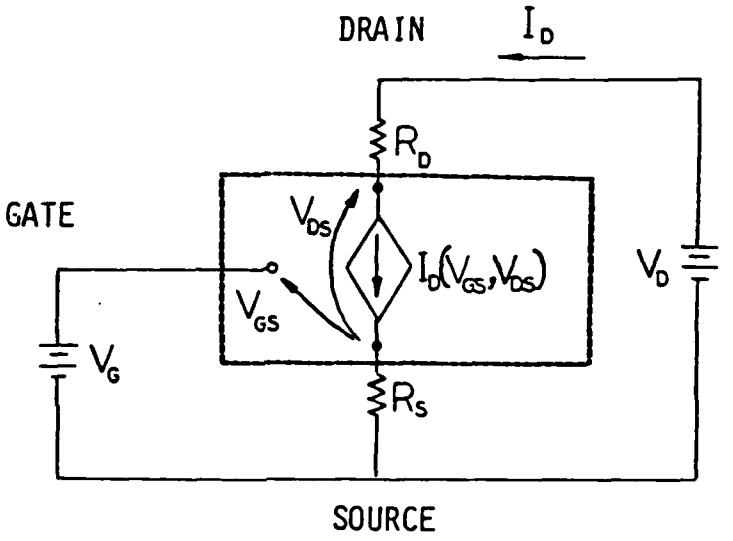


Figure 2.1 Circuit model used to calculate static drain current characteristics.

determine I_D as a function of the external terminal voltages V_D and V_G. This is accomplished by writing the Kirchoff voltage law equations for the circuit and solving them using a Newton-Raphson algorithm (39). This results in values for V_1, V_2, I_D and the other model output quantities.

2.1.1 Determination of R_S and R_D.

Spreading and contact resistance effects are difficult to calculate. The spreading resistance can be approximated (28), but the contact resistances are more difficult to predict. They depend upon processing techniques and tend to vary from transistor to transistor. Consequently, it was decided to obtain R_S and R_D through comparison of measured I-V characteristics with the calculated ones. This is done by assuming that $R_S=R_D$, and comparing g_D and g_M calculated by the basic model (which excludes R_S and R_D) with values measured from experimental I-V characteristics. The two are compared at $V_D=0$ and $V_G=0$. Here, V_D is selected near zero volts so that there is no appreciable current carried by the transistor which would complicate the comparison by introducing nonlinear thermal effects. The applied gate voltage, V_G, is chosen to be zero so that the g_D's will be large for more ease in measurement. An incremental version of the static circuit

is shown in Figure 2.2. Here we have:

$$I_D = g_M V_1 + g_D V_2$$

$$= g_M(V_G - R_S I_D) + g_D[V_D - (R_S + R_D) I_D]$$

assuming $R_S = R_D = R$,

$$G_{Dext} = \frac{dI_D}{dV_G} = g_D / [1 + R(g_M + 2g_D)]$$

so:

$$R = [(g_D / G_{Dext}) - 1] / (g_M + 2g_D)$$

Figure 2.3 compares calcuated and measured I-V characteristics for the 1.7 micron gate length MESFET described in Table 2.1. Predicted and measured results are in agreement for low values of V_D, but diverge significantly in areas of the I-V plane which correspond to higher levels of power dissipation, and consequently higher device temperatures.

2.1.2 Temperature Effects

Neidert has conducted an extensive literature survey of published experimental and theoretical values for electron mobility in n-type GaAs as a function of doping

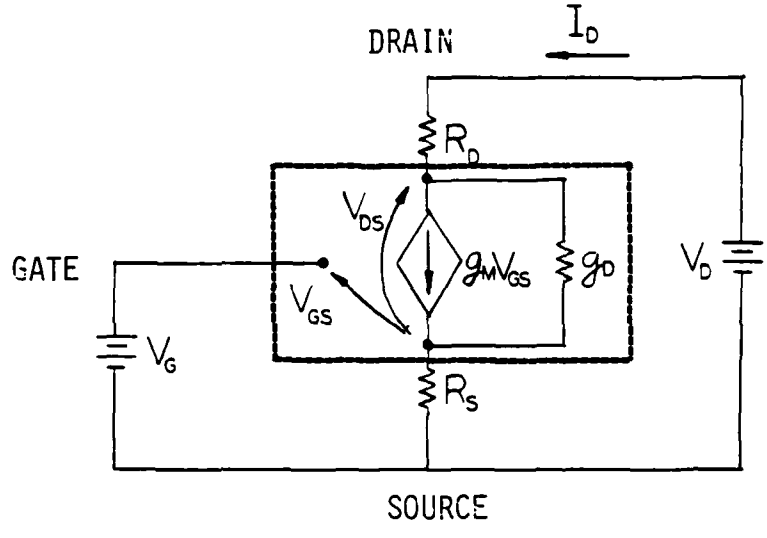


Figure 2.2 Incremental static circuit model used to estimate R_S and R_D by comparing measured drain current characteristics with basic nonlinear MESFET model calculated results.

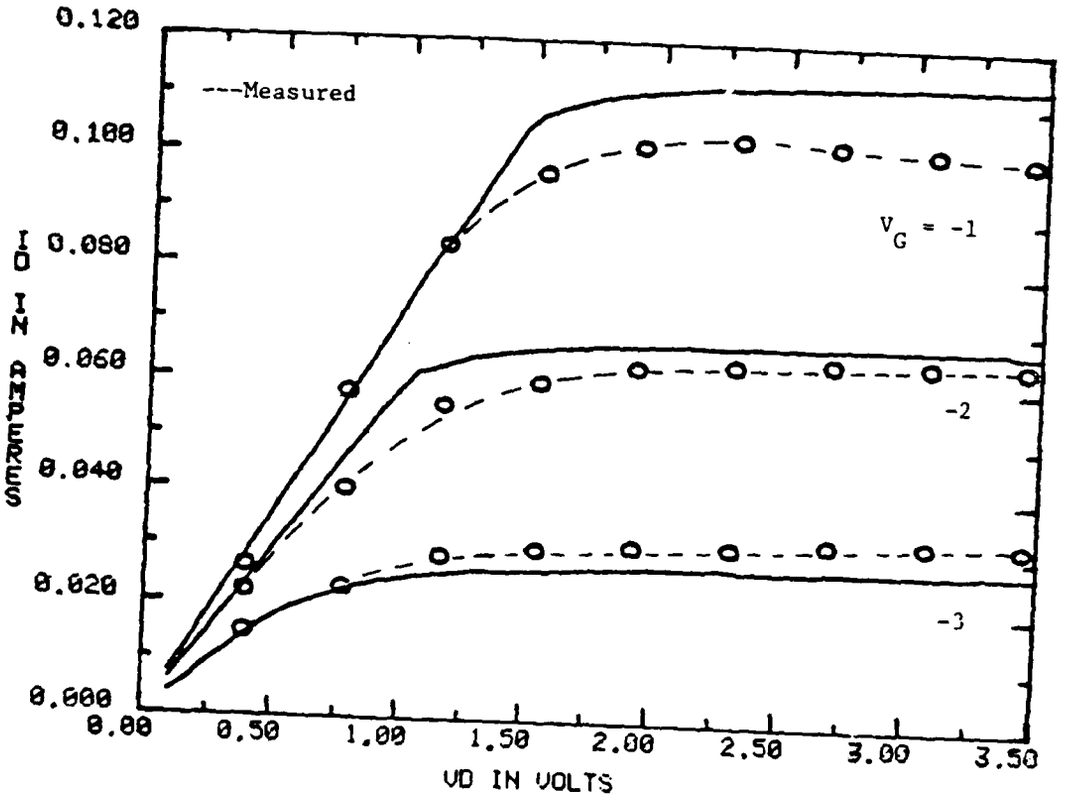


Figure 2.3 Calculated and measured common-source static drain current characteristics for the MESFET described in Table 2.1. The temperature for the calculations was 300 K.

Device Parameters

Gate-Source Spacing	(ℓ_{gs}):	1.7 μm
Gate Length	(ℓ_g):	1.7 μm
Gate-Drain Spacing	(ℓ_{gd}):	1.7 μm
Gate Width	(W):	600 μm
Epitaxial Layer Thickness	(a):	0.3 μm
Doping Density	(N_D):	7.5×10^{16} cm^{-3}
Critical Electric Field	(E_c^l):	3.2 KV/cm
Saturated Velocity	(v_s^l):	1.36×10^7 cm/sec
Relative Dielectric Constant	(ε_r):	12.5
Built-in Potential	(V_{bi}):	0.7 V

Table 2.1 Geometric and material parameters used to model a developmental Texas Instruments GaAs MESFET.

level and temperature , and has derived an approximate relation for low-field mobility as a function of temperature (40):

$$\mu_0 = \mu_0\Big|_{300K}\left[\frac{300K+R_{TH}P_D}{300K}\right]^{-0.7} \qquad (2.2)$$

where μ_0 is low field mobility, R_{TH} is the thermal resistance of the transistor, and P_D is the total power dissipated in the transistor. This relation holds for a doping level of the order of 10^{17} cm^{-3}, which is typical for a microwave MESFET, and for temperatures above 300 K.

The electron velocity-field relationship used by Yamaguchi and Kodera in the numerical simulations upon which they base their model (26) is the piecewise linear Curve A in Figure 2.4. It was discovered by Madjar and Rosenbaum (28) that the use of this curve in their model resulted in static drain current characteristics that retained the piecewise linear nature of the velocity-field relationship, resulting in drain current that increased approximately linearly with drain-source voltage, and abruptly became constant with the onset of current saturation. In order to eliminate discontinuities in the slopes of the I-V characteristics, a parabolic approximation (Curve B in Figure 2.4) to the

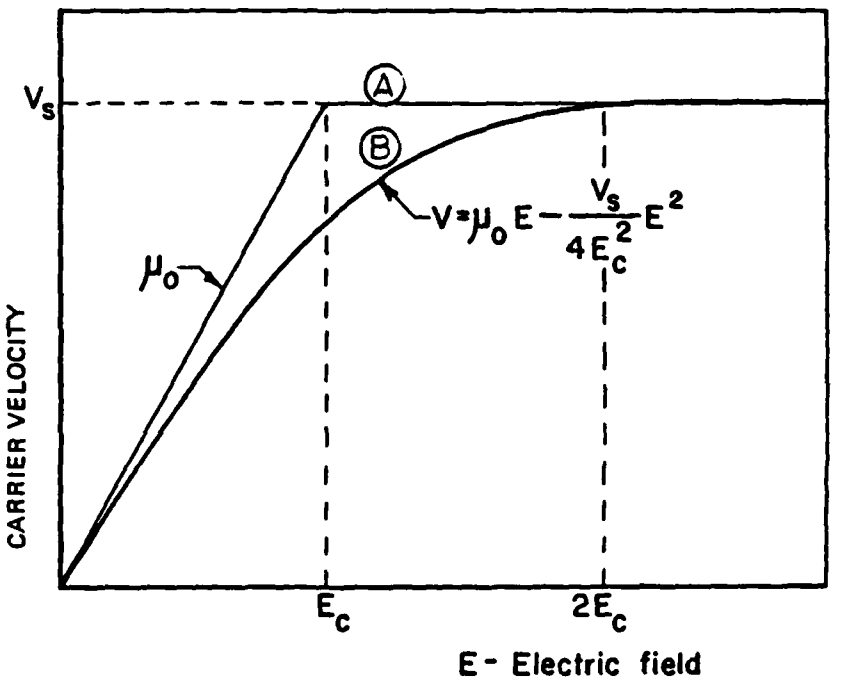


Figure 2.4 Electron velocity-field relations used in the Yamaguchi-Kodera FET simulations (Curve A), and in the Madjar-Rosenbaum MESFET model (Curve B).

velocity-field curve was used which has the same low field mobility and saturated velocity as the piecewise linear relation used by Yamaguchi and Kodera. In both cases, the saturated electron velocity is proportional to low field mobility for fixed critical electric field. Because the critical electric field for GaAs is relatively insensitive to temperature, Neidert's relation can be adapted to modify the saturated electron velocity, which is used as an input to the Madjar-Rosenbaum basic nonlinear MESFET model. The modified relation that is used here is:

$$V_S = V_S\Big|_{300K}\left[\frac{300K+R_{TH}P_D}{300K}\right]^{-0.7} \qquad (2.3)$$

Static drain current characteristics suitable for comparison with experimental results must be calculated taking into account the MESFET temperature corresponding the the power dissipation level under a particular operating condition. At higher drain-source voltages and drain currents, the degradation of electron velocity due to higher channel temperatures can result in decreasing drain current with increasing drain-source voltage, i.e. negative G_D. Common-source static drain current characteristics measured for the 0.5 micron gate-length transistor described in Table 2.2 and illustrated in

NEC NE869177 MESFET
CONSTRUCTION PARAMETERS
USED AS INPUT TO MODEL

GATE LENGTH:	0.5 microns
GATE WIDTH:	750 microns
EPI LAYER THICKNESS*:	0.21 microns
N_D*	1.75×10^{17} cm^{-3}
THERMAL RESISTANCE:	100° c/w

*Not available from manufacturer, obtained from C-V measurements.

Table 2.2 Geometric and material parameters for the NE869177 MESFET.

Figure 1.2 are shown in Figures 2.5 and 2.6. The characteristics of Figure 2.5 were measured on a curve tracer in which the drain-source voltage was cycled at 60 Hz. The MESFET was mounted in a simple probing station with no special care taken to control the microwave impedances of the circuit. There is looping in the characteristics, and low frequency oscillations also occur for some bias voltages. Figure 2.6 shows more carefully taken measurements on the same type of transistor, but this time manually, with adequate time allowed to achieve thermal equilibrium at each pair of drain-source and gate-source voltages. Constant power dissipation contours are also shown in the figure. This time, the transistor was mounted in a microstrip circuit with the drain-source and gate-source ports terminated with matched loads. Microwave power generated by the MESFET was monitored with a power meter and spectrum analyzer. The data points indicated by the triangles in Figure 2.6 correspond to bias voltages at which microwave power was detected, and so the measured D.C. current is an average, rather than a static value. The source of this oscillation is probably related to Gunn instabilities which will be discussed in the next section.

For the calculation of a set of characteristics such as this, measured at multiple temperatures, the use of the temperature corrected MESFET model would be time

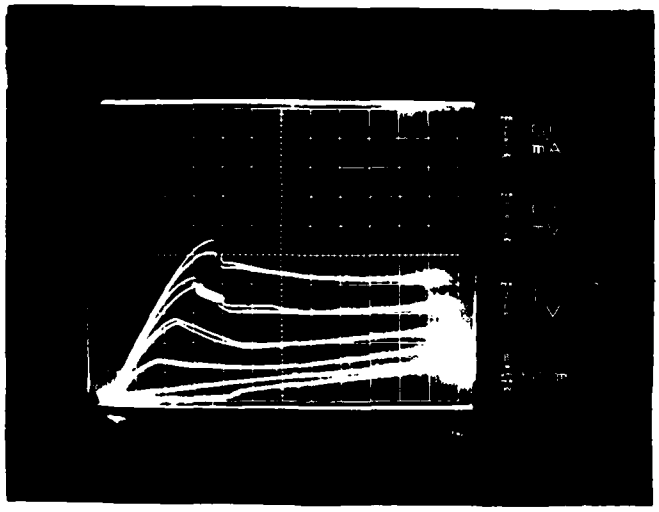


Figure 2.5 Common-source drain current characteristics for the NE869177 MESFET measured on a curve tracer which cycled the drain-source voltage at 60 Hz.

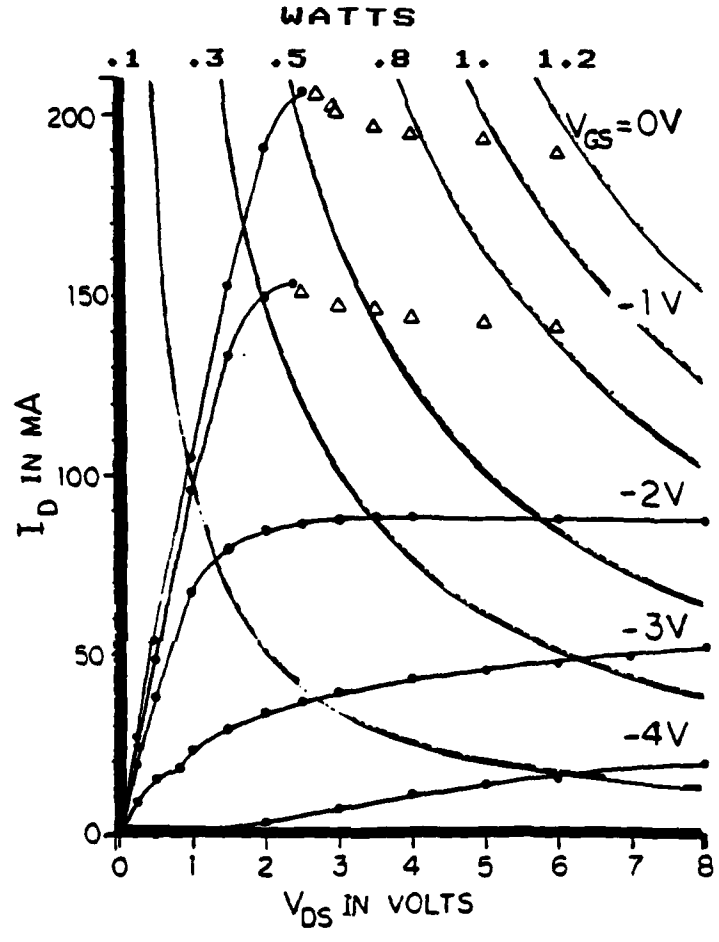


Figure 2.6 Common-source static drain current characteristics for the NE869177 MESFET, mounted in a microwave circuit and measured on a point-by-point basis to allow time for thermal equilibration. Also shown are constant power dissipation contours.

consuming. For each point, the drain current would need to be calculated using an initial guess for the device temperature, according to the technique described in Section 2.1. Power dissipation and device temperature could then be calculated, and the procedure repeated until convergence is obtained.

Figure 2.7A is a comparison of experimental and temperature corrected modeled drain currents as functions of gate-source voltage for fixed drain-source voltage. In this case, the experimental results were obtained first, and the measured power dissipation was used to determine the saturated electron velocity used as input to the model. The two curves are in good agreement. Figure 2.7B is a similar comparison, but with the model temperature fixed, at the experimentally determined power dissipation level for V_{GS}=-3 V. As expected, the error is largest for the smaller gate-source voltages which result in higher drain currents and power dissipation levels. Overall, the agreement with experimental results is superior for the temperature corrected model.

In large-signal microwave applications the MESFET operates isothermally, at a temperature related to the average power dissipated over one microwave period. Hence, static characteristics which are not measured isothermally, are not appropriate for large-signal microwave circuit applications. Figure 2.8 shows

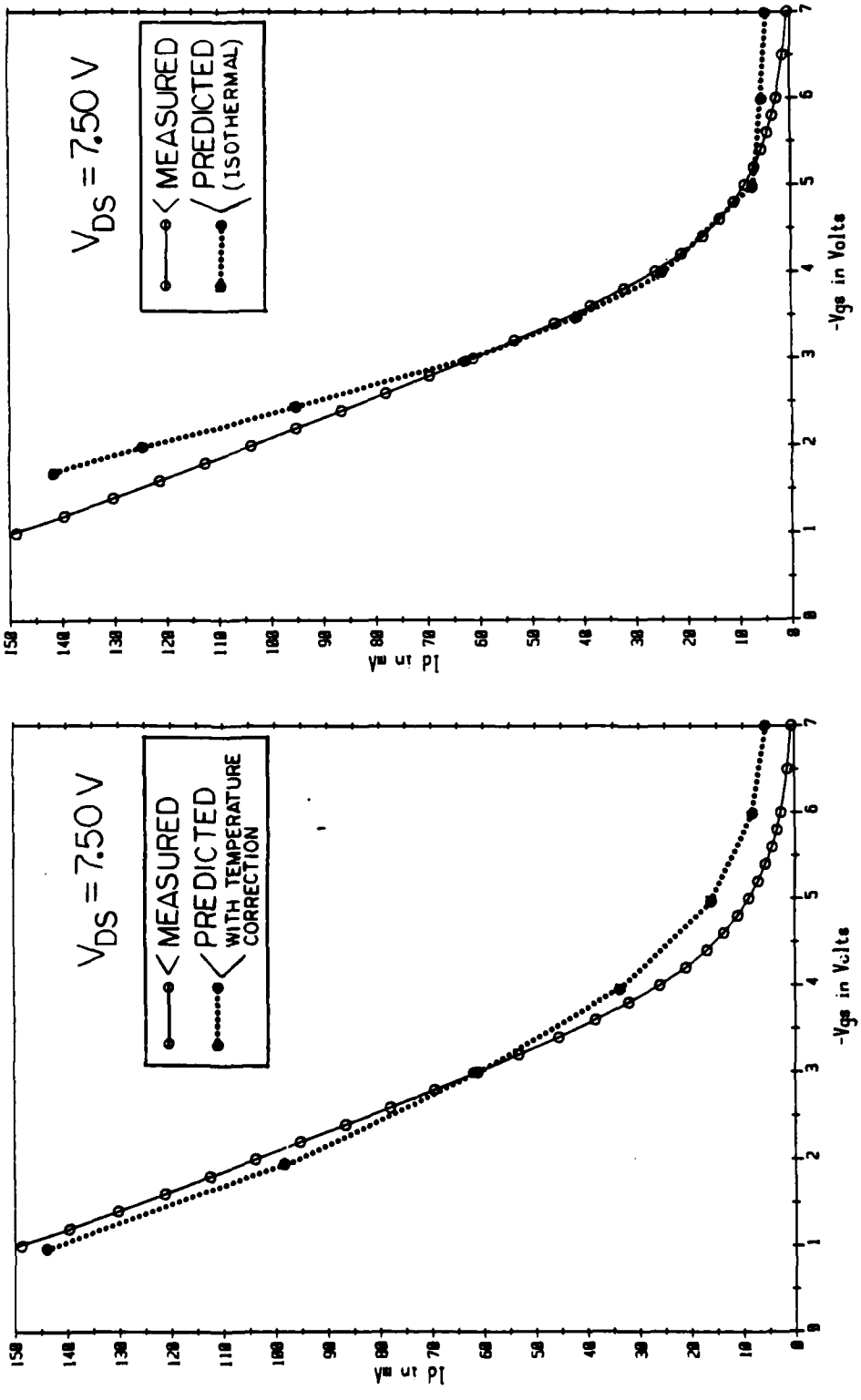


Figure 2.7 Measured and calculated drain current for the NE869177.

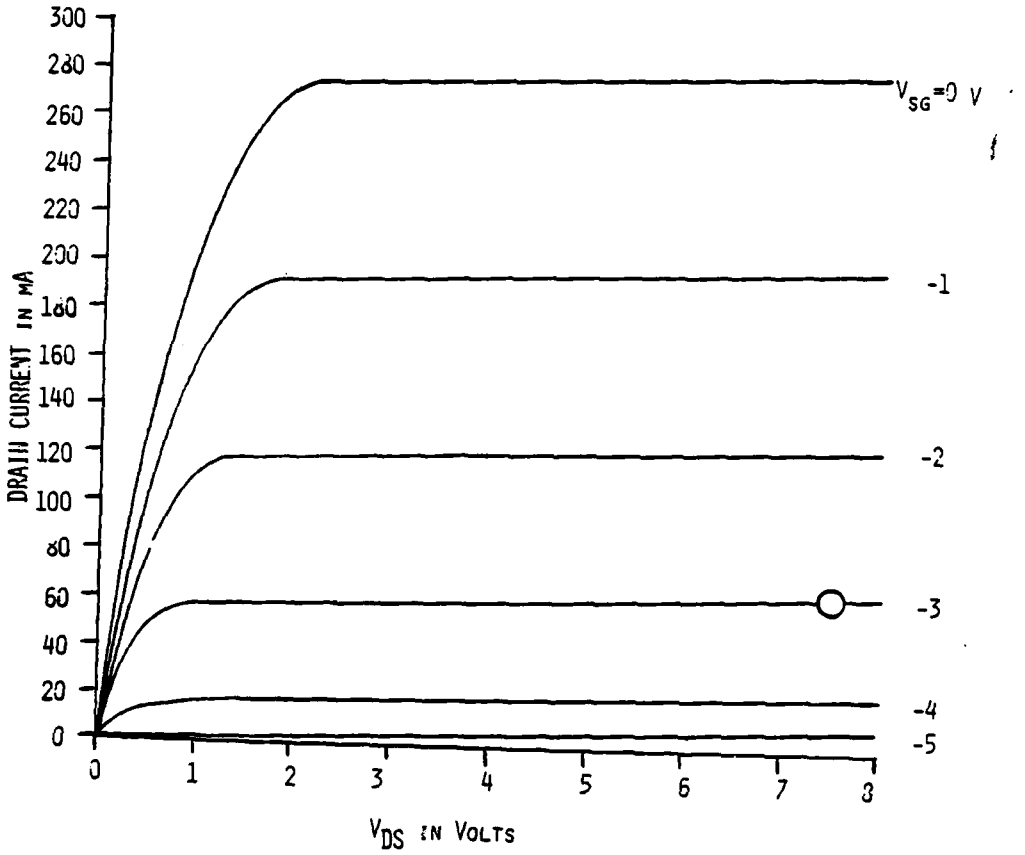


Figure 2.8 Calculated static isothermal drain current characteristics for the NE869177 MESFET. The temperature corresponds to the power dissipation level indicated by the open circle.

isothermal static drain characteristics for the NE869177 which were calculated using the MESFET model. The temperature corresponds to the power dissipation level indicated by the open circle in the I-V plane. Incremental values from these curves will be used in the modeling of some of the S-parameters in Section 2.2.

The modeled isothermal characteristics do not exhibit any negative G_D or indicate bias ranges for potential Gunn instabilities. A discussion of these phenomena and their relationship to the omission of negative differential mobility in the original Yamaguchi and Kodera simulations follows in the next section.

2.1.3 Negative Differential Mobility and Charge Accumulation Effects.

The electron velocity-field relation (V(E) curve) used by Yamaguchi and Kodera to develop their FET model (26) is shown in Figure 2.4A, and does not include negative differential mobility. However there is such a region in the V(E) curve for GaAs. This can result in Gunn instabilities (30) and possibly other effects. In a subsequent paper, Yamagacuhi, Asai and Kodera (23) reported a limited number of two-dimensional MESFET simulations using a V(E) relation proposed by Thim (41):

$$V(E) = \frac{\mu_0 E + V_S (E/E_0)^4}{1+(E/E_0)^4} \qquad (2.4)$$

where E is the magnitude of the electric field, μ_0 is the low field mobility, V_S is the saturated velocity, and E_0 is the saturation field. The region of negative differential mobility can be seen in Figure 2.9.

Yamaguchi et. al. (23) came to the conclusion that MESFETs fabricated on thick n-type GaAs layers could exhibit Gunn oscillations. This conclusion is supported by simulations and experiments conducted by Grubin, Ferry and Gleason (42), who more succintly state the criterion for potential current instabilities as

$$I_{DSS} > G_0 * E_S * L ,$$

where I_{DSS} is the saturated drain current at zero gate-source bias, G_0 is the open channel conductance, E_S is the ratio of the saturated electron velocity to the low field mobility, and L is the source to drain separation. MESFETs fulfilling this criterion are subject to Gunn effect current instabilities at gate-source biases near zero volts. This is a condition sometimes encountered in GaAs MESFETs intended for power applications.

Another result of the Yamaguchi et. al. simulations (23) was the prediction of a region of static negative

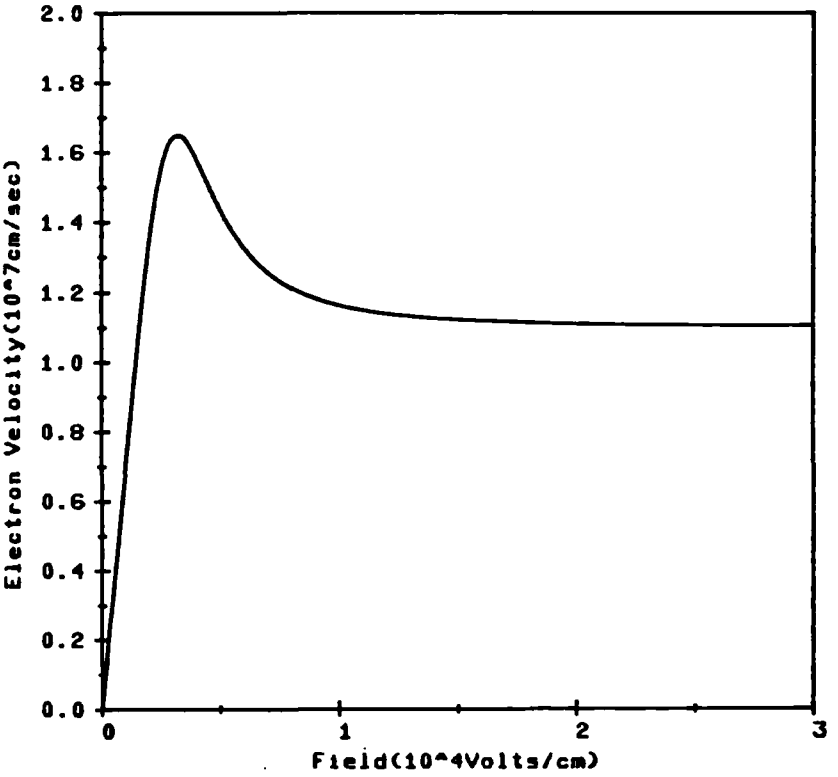


Figure 2.9 Electron velocity-field relation for GaAs, calculated using Thim's equation (2.4), for the case: μ_0 = 6875 $cm^2/(V*sec)$, E_0 = 3200 V/cm, and v_S = 1.1 x 107 cm/sec.

differental resistance in isothermal common-source drain current characteristics. They call this "stable negative resistance (SNR)". They attribute SNR to a charge accumlation phenomenon in the MESFET channel near the drain side of the gate, which is somehow related to negative differential mobility. SNR is prominent in the same region of the I-V characteristics that exhibits the maximum negative G_D due to thermal effects (Figure 2.6). This gives rise to the possibilty of ambiguous interpretation of I-V data taken under nonisothermal conditions. Pulsed I-V characteristics measured by Grubin et. al. (42) of MESFETs in isothermal operation do not indicate any regions of static negative resistance, even though they do exhibit Gunn instabilities at small gate-source biases.

This raises the possibility that the SNR of Yamaguchi et. al. may be a numerical artifact of the two-dimensional finite difference algorithm (23) that they used. SNR was observed only in the simulations that, for simplicity, assumed a perfectly insulating substrate. SNR was not observed in simulations with nonzero substrate conductivity. More recently, Norton and Hayes (43) have replicated some of the questioned simulations, and have expressed their opinion that the SNR is the result of an inadequately small mesh size. This observation has been criticized by Laux and Lomax (44).

It is appealing to try to avoid this controversey over numerical methods by resorting to more fundamental arguments. It should first be observed that charge accumulation, i.e. electron concentration greater than the doping level, is seen in two-dimensional simulations of silicon FETs (20), and thus does not require negative differential mobility. Secondly, one must consider Shockley's negative resistance theorem, which can be paraphrased: "negative differential mobility cannot result in static negative resistance." As originally demonstrated by Shockley (45), the derivation was one-dimensional and neglected diffusion. It was further generalized to include constant diffusion and arbitrary two-dimensional geometries and doping profiles by Kroemer (46). Consideraton of specific field dependent diffusion curves generally requires a numerical solution of the partial differential equations involved. A numerical investigation by Hauge (47) indicated that some velocity-field and diffusion-field curve combinations might result in static negative differential resistance; however shortly afterward, Dohler (48), using theoretical arguments, demonstrated that Hauge's solutions could not be time invariant (i.e. static) and thereby completed the generalization of Shockley's negative resistance theorem.

Because Shockley's negative resistance theorem holds, and since the assumptions in the Yamaguchi et. al.

analysis (23) preclude the possibility of tunneling effects (49), we are left with only one additional potentially valid explanation for SNR, namely some voltage or current feedback effect resulting from a combination of static characteristics which do not, individually, exhibit static negative resistance. Wu and Wu (50) have conducted an extensive investigation of circuit topologies combining three-terminal elements with FET-like characteristics, in order to obtain static negative resistance across a pair of circuit nodes. Their analysis indicates that such a circuit can only be realized if it contains no fewer than two FET-like elements which are interconnected in ways that bear no resemblance to any conceivable conceptual partitioning of a single MESFET. This casts doubt on possible feedback hypotheses that might explain static negative differential resistance in the Yamaguchi et. al. (23) simulations.

Inspired by the Yamaguchi et. al. SNR results, many papers have been published attempting to model the charge accumulation region in MESFETs fabricated from negative differential mobility semiconductors as "stationary Gunn domains" , and calculate effects on MESFET behavior (51-54). Several of these papers (51-53), are based on Shur and Eastman's analytic model (27) which gives the voltage across the "stationary Gunn domain" as a function of the magnitude of the electric field at the drain side

of the region under the gate. Unfortunately when the analysis is traced back through two of Shur's earlier publications (55,56), it is discovered that it includes the assumption that the high field Gunn domain moves at the same velocity as the carriers outside the domain. This is the same assumption that permits derivation of the "Equal Areas Rule" (57) for traveling domains in classical Gunn device theory. This seems to be a somewhat strained approximation for the stationary charge accumulation phenomenon seen in numerical two-dimensional MESFET simulations, where the carriers outside the "domain" are moving to support the drain conduction current.

An exhaustive attempt was made earlier by this author to use the Shur and Eastman "static Gunn domain model" in conjuncton with the Madjar-Rosenbaum basic nonlinear MESFET model. The result was an inherent discontinuity in the static drain current characteristics, and saturated drain currents that were too low (Figure 2.10). The reason for the discontinuity is demonstrated in Appendix 8.1.

Willing and de Santis (54) have included a negative resistance element in an equvalent MESFET circuit used for the bias-dependent small-signal S-parameter MESFET modeling technique described in Section 1.2.1. In addition to using this element to account for static negative GD, they simultaneously used it to account for

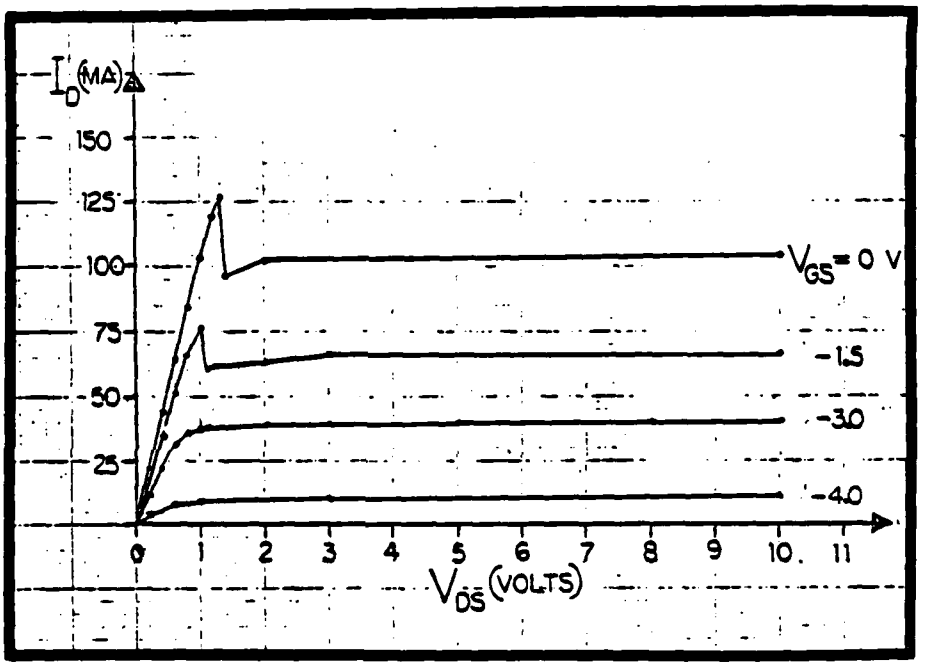


Figure 2.10 Static drain current characteristics for the Texas Instruments MESFET, using the "stationary Gunn Domain" correction proposed by Shur and Eastman (27).

measured reflection coefficients for the drain-source port of the transistor which are greater than one. This reflection gain could theoretically result from static negative G_D, but it could also result from travelling Gunn domain effects such as are utilized in Gunn diode amplifiers (30). The connection between the reflection gain at microwave frequencies and the apparent static negative G_D (from nonisothermal measurements) appears to be coincidental.

In view of these theoretical considerations and experimental results, we have chosen not to incorporate static negative G_D in our MESFET modeling. Although velocity saturation exerts a strong influence on the calculated saturated drain conduction current predicted by the model, negative differential mobility appears to play a role in the static characteristics only at the onset of Gunn instabilities in the drain current, in which case static characteristics are no longer applicable, and the MESFET is not useful in a conventional sense. This does not mean, however, that the charge accumulation region is not important in MESFET behavior, as it may affect the nonlinear feedback capacitance (58) and play a role in breakdown mechanisms as well. The Madjar-Rosenbaum model includes a phenomenological representation for the effects of charge accumulation at the drain side of the gate.

2.1.4 Substrate Current

The Yamaguchi-Kodera FET model which was described in Section 1.1.3 does not include substrate current effects, and consequently, neither does the Madjar-Rosenbaum model. Whether or not a substrate current correction is necessary for a specific transistor is determined by examining the experimental common-source I-V characteristics. The slope of the cut-off drain current is used to determine the value of a linear resistance which is placed across the drain and source terminals of the nonlinear current source in Figure 2.1. For the NE869177 MESFET (Table 2.2), the value of this resistance has been found to vary from one thousand ohms to fifty ohms, depending on the particular device under test. The lower substrate resistances were observed to be gate-source voltage dependent, and were avoided in the experiments that are reported here. Because of the lack of uniformity among the same model of transistor due to the apparent sensitivity of substrate current effects to substrate preparation and n-type layer - substrate interface phenomena, it was decided not to pursue substrate current modeling in greater depth than including a linear resistance.

Eastman and Shur (51) have developed a model for substrate current in GaAs MESFETs based on their "static

Gunn domain" theory (27). Unfortunately this theory predicts minimum substrate current when the channel is pinched off, and this is the opposite of what is observed experimentally.

2.2 SMALL-SIGNAL S-PARAMETER CALCULATION.

The incrementally linear version of the MESFET model with package parasitics that is used for the calculation of small-signal S-parameters is shown in Figure 2.11. R_S and R_D are the source and drain combined contact and spreading resistance that were described in Section 2.1. R_G is a gate metallization resistance. C_{GS1} and C_{DS1} are bonding pad capacitances. L_S, L_G, and L_D are lead inductances. C_{GS2} and C_{DS2} are microstrip fringing field capacitances associated with the microstrip test fixture in which the transistor is mounted for comparison measurements.

The dashed box contains incremental elements from the basic nonlinear model. An alternative version of this innermost part of the network which replaces the nonlinear gate charging resistance, R_C, with a time delay in the control voltage, V_1, is shown in Figure 2.12. The motivation for the alternative representation will be discussed in Chapter 4. Both versions result in essentially identical calculated S-parameters.

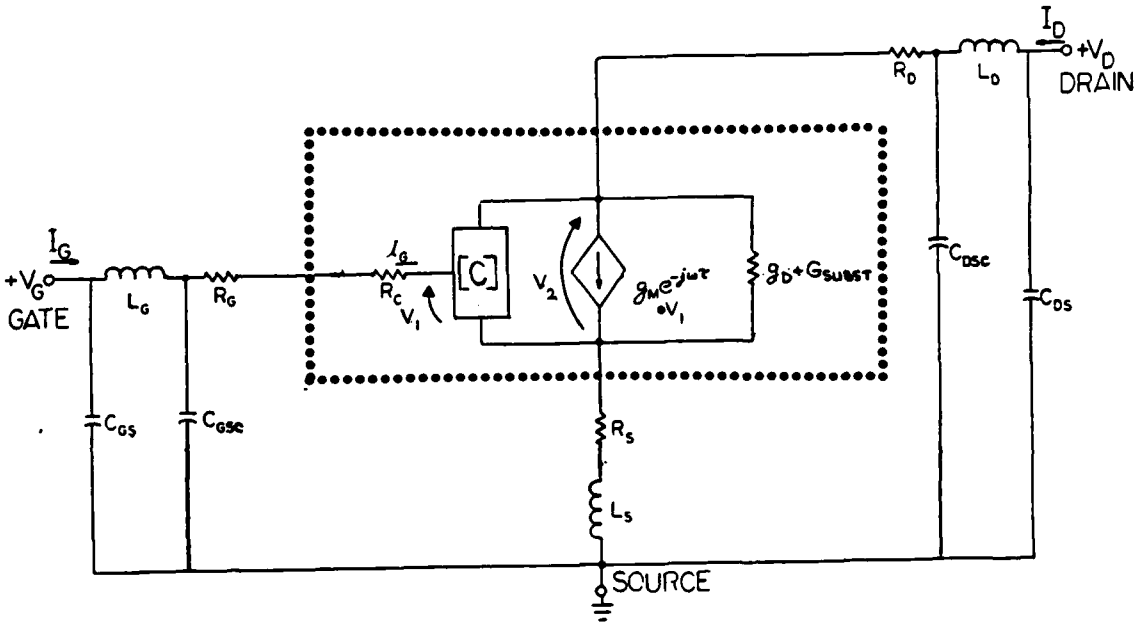


Figure 2.11 Incrementally linear packaged MESFET model for small-signal scattering parameter calculations using the gate charging resistance, R_C.

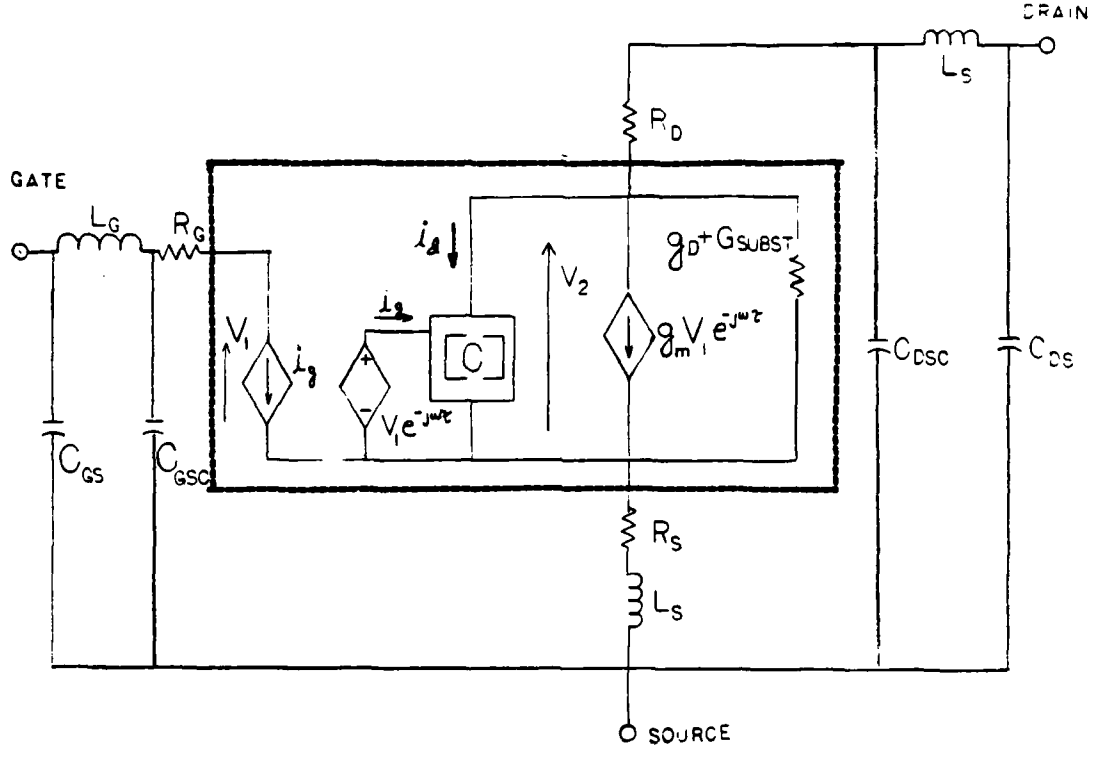


Figure 2.12 Incremental version of the basic nonlinear MESFET model with the gate charging resistance replaced by a time delay in the control voltage, V_1.

The following sequence is used to calculate the S-parameters:

1.) The basic nonlinear model is used with the Newton-Raphson algorithm which was described in Section 2.1, in order to determine the incremental values for the nonlinear elements corresponding to the specified external bias voltages.

2.) The complex admittance matrix for the nonlinear network is calculated.

3.) The admittance matrix is inverted and RG and RD are added to the resulting impedance matrix.

4.) The impedance matrix is inverted, and the shunt capacitances C_{GS1} and C_{DS2} are added to the resulting admittance matrix.

5.) The admittance matrix is inverted and the series inductances and resistances L_S, L_G, L_D, and RS are added to the resulting impedance matrix.

6.) The impedance matrix is inverted and the shunt capacitances C_{DS2} and C_{GS2} are added to the resulting admittance matrix.

7.) The admittance matrix is normalizd to 50 ohms and converted to the scattering parameter matrix.

Common-source scattering parameters for the NE869177 MESFET (described in Table 2.2 and illustrated in Figure 1.2) were measured on an automatic microwave network

analyzer. The source and drain microstrip tuning stubs pictured in Figure 1.2 were removed to simplify network analyzer calibration. The measured results are shown over a 3 to 11 GHz frequency range in Figures 2.13 through 2.16 for V_{GS}=-3 V, which results in a drain current which is about one half of the zero voltage gate bias saturated drain current; and in Figures 2.17 through 2.20 for V_{GS}= -6 V, where the transistor is cut-off.

Initial estimates for parasitic element values were based on manufacturer-supplied information (59). The measurements taken with V_{GS}=-3 V were then used as a guide in the manual refinement of the parasitic reactance values presented in Table 2.3. These values were then used with the MESFET model (the version without R_C) to calculate the S-parameters which are also displayed in Figures 2.13 through 2.20. Incremental values for the nonlinear elements calculated by the basic MESFET model are shown in Table 2.4. The match is reasonable when the precision of the S-parameter measurements is considered, and it tracks the change in bias voltage. Vendelin and Omori (60) have described a computer technique for the automatic determination of parasitic element values which could result in an even better match between predicted and measured results.

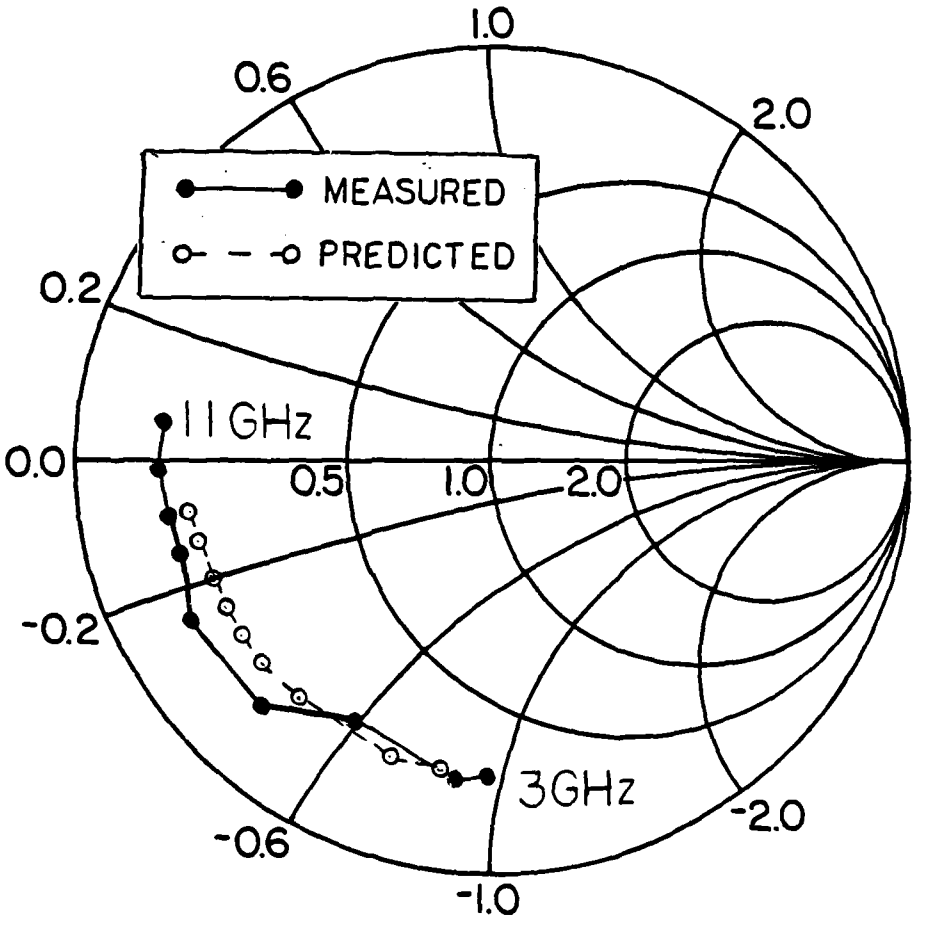


Figure 2.13 Predicted and measured S_{11} for the NE869177 MESFET. Bias: V_{DS} = 7.50 volts, V_{GS} = -3.00 volts.

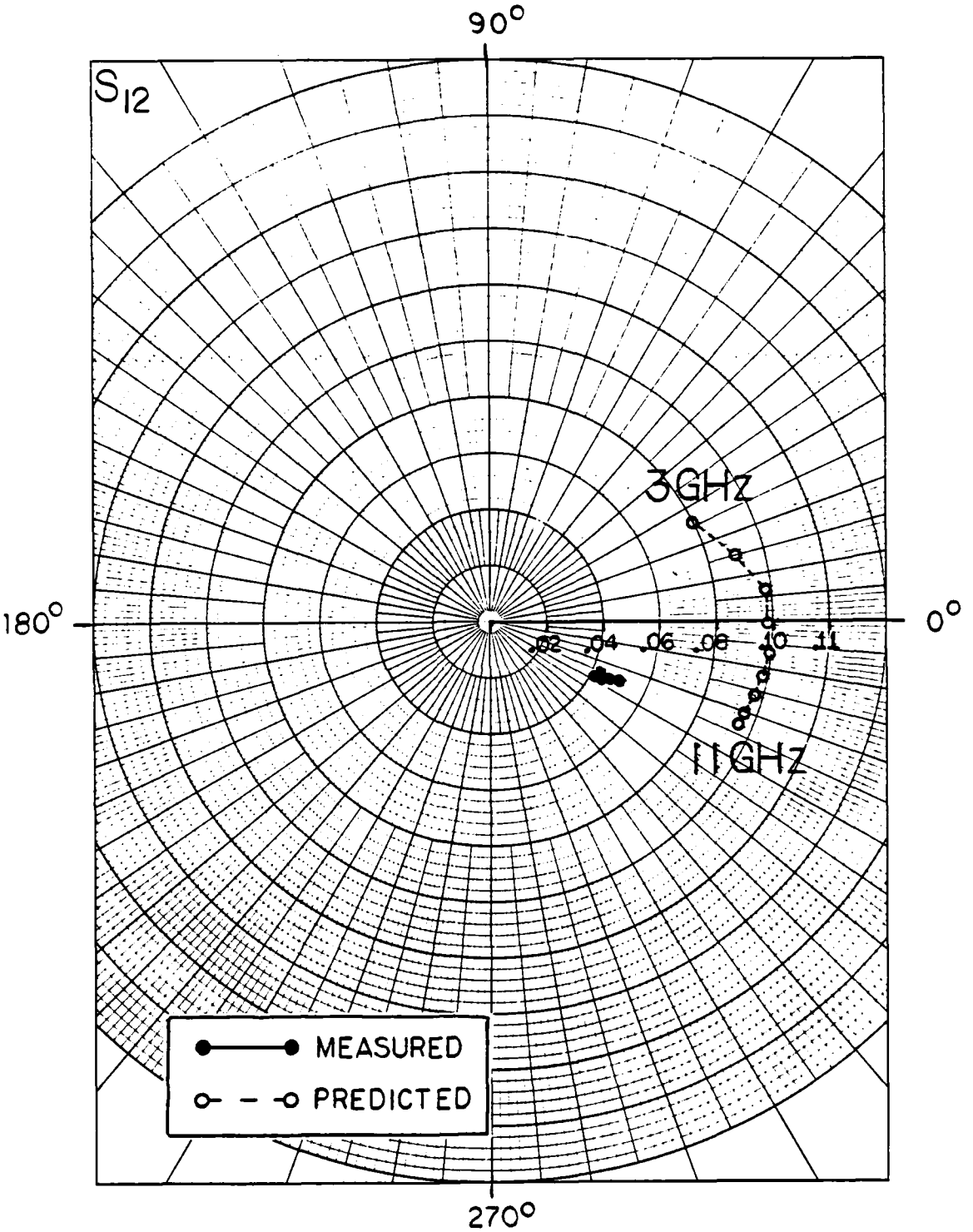


Figure 2.14 Predicted and measured S_{12} for the NE869177 MESFET. Bias: V_{DS} = 7.50 volts, V_{GS} = -3.00 volts.

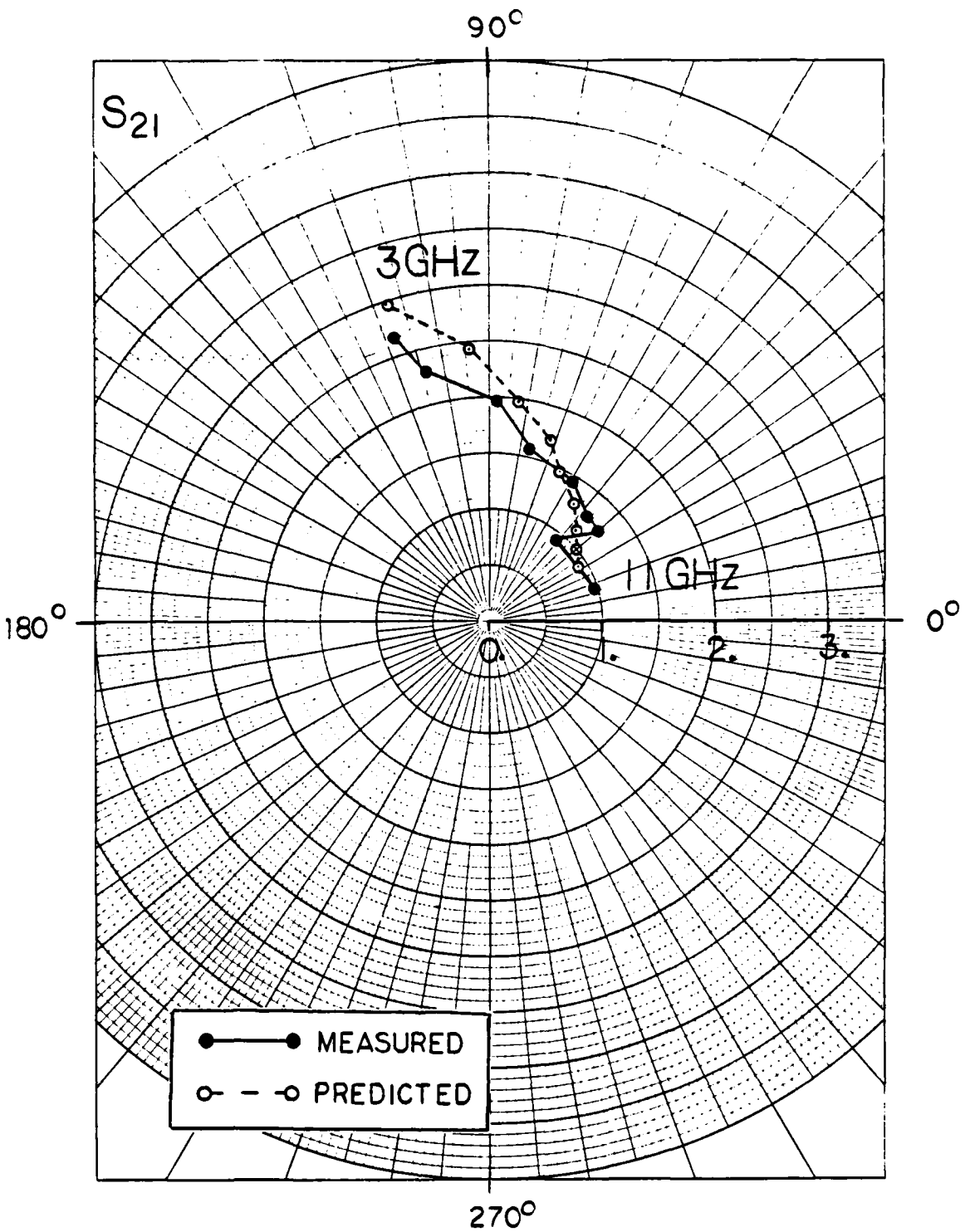


Figure 2.15 Predicted and measured S_{21} for the NE869177 MESFET. Bias: V_{DS} = 7.50 volts, V_{GS} = -3.00 volts.

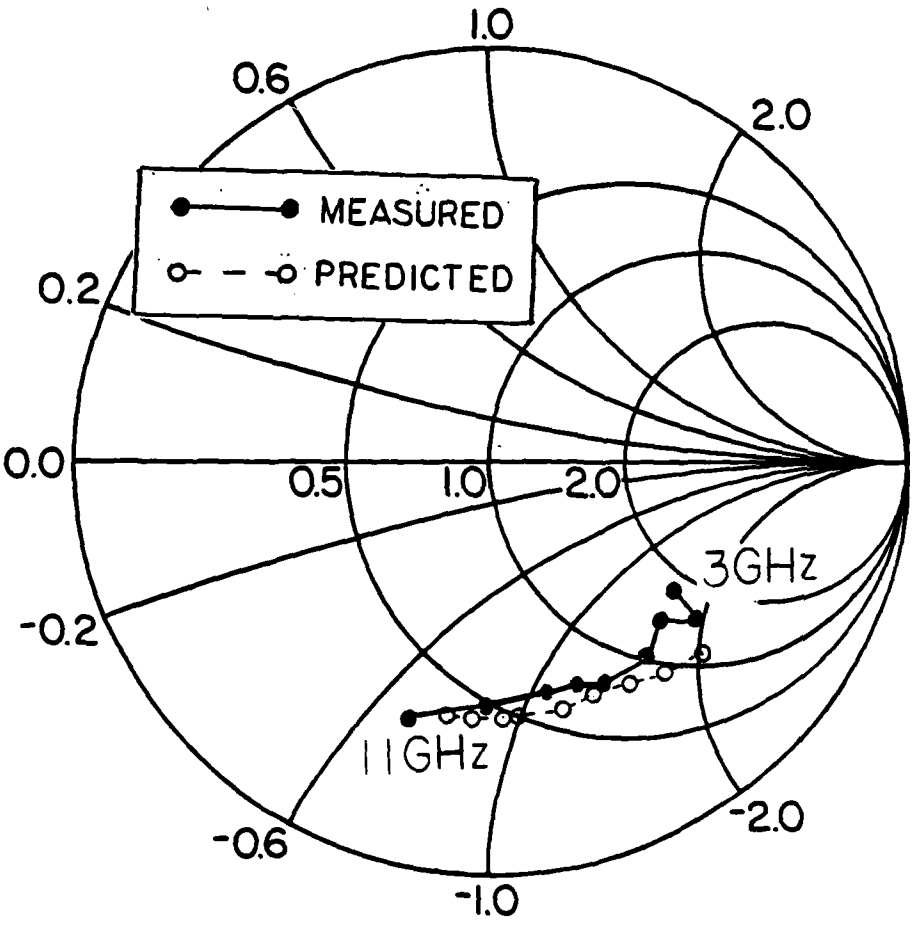


Figure 2.16 Predicted and measured S_{22} for the NE869177 MESFET. Bias: V_{DS} = 7.50 volts, V_{GS} = -3.00 volts.

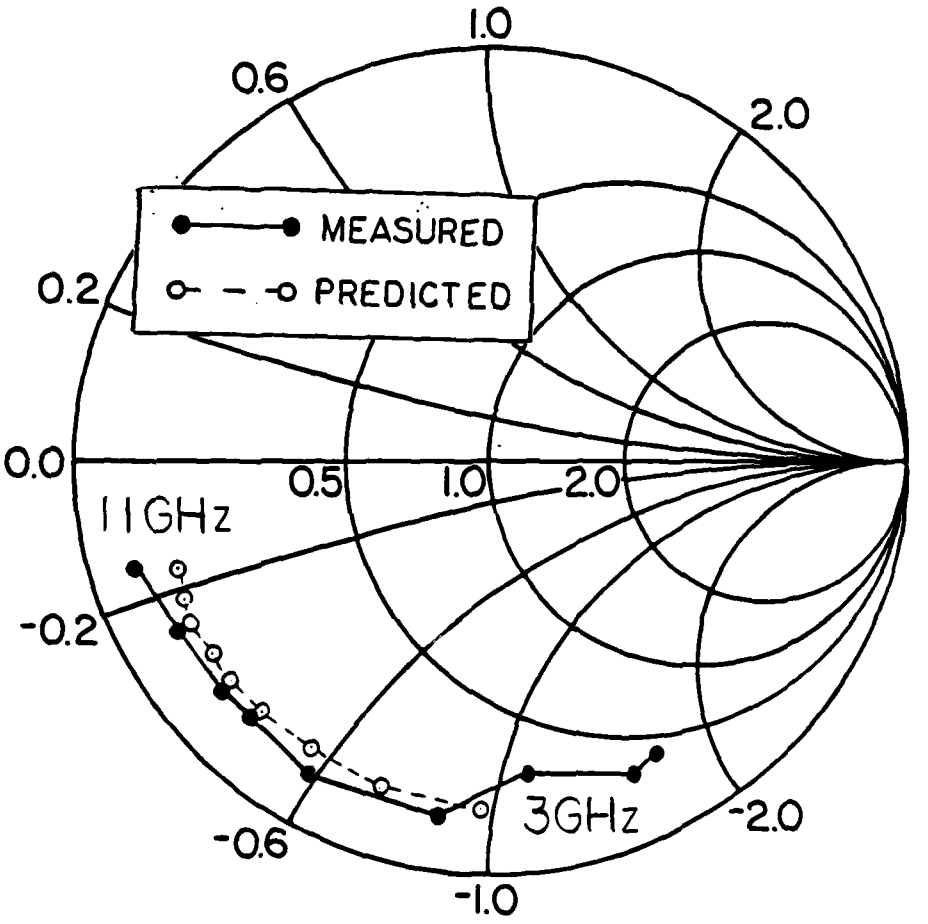


Figure 2.17 Predicted and measured S_{11} for the NE869177 MESFET. Bias: V_{GS} = 7.50 volts, V_{GS} = -6.00 volts.

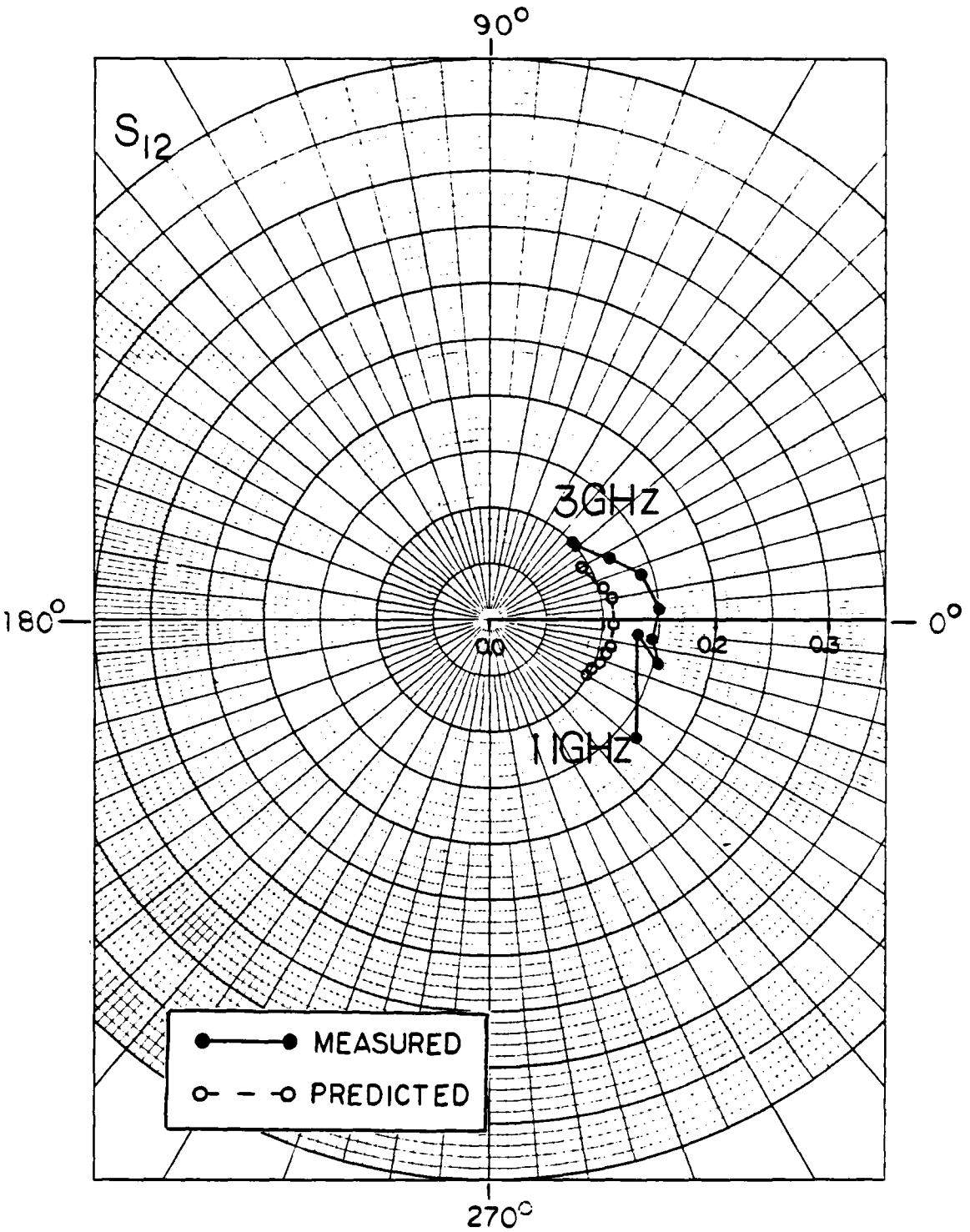


Figure 2.18 Predicted and measured S_{12} for the NE869177 MESFET. Bias: V_{GS} = 7.50 volts, V_{GS} = -6.00 volts.

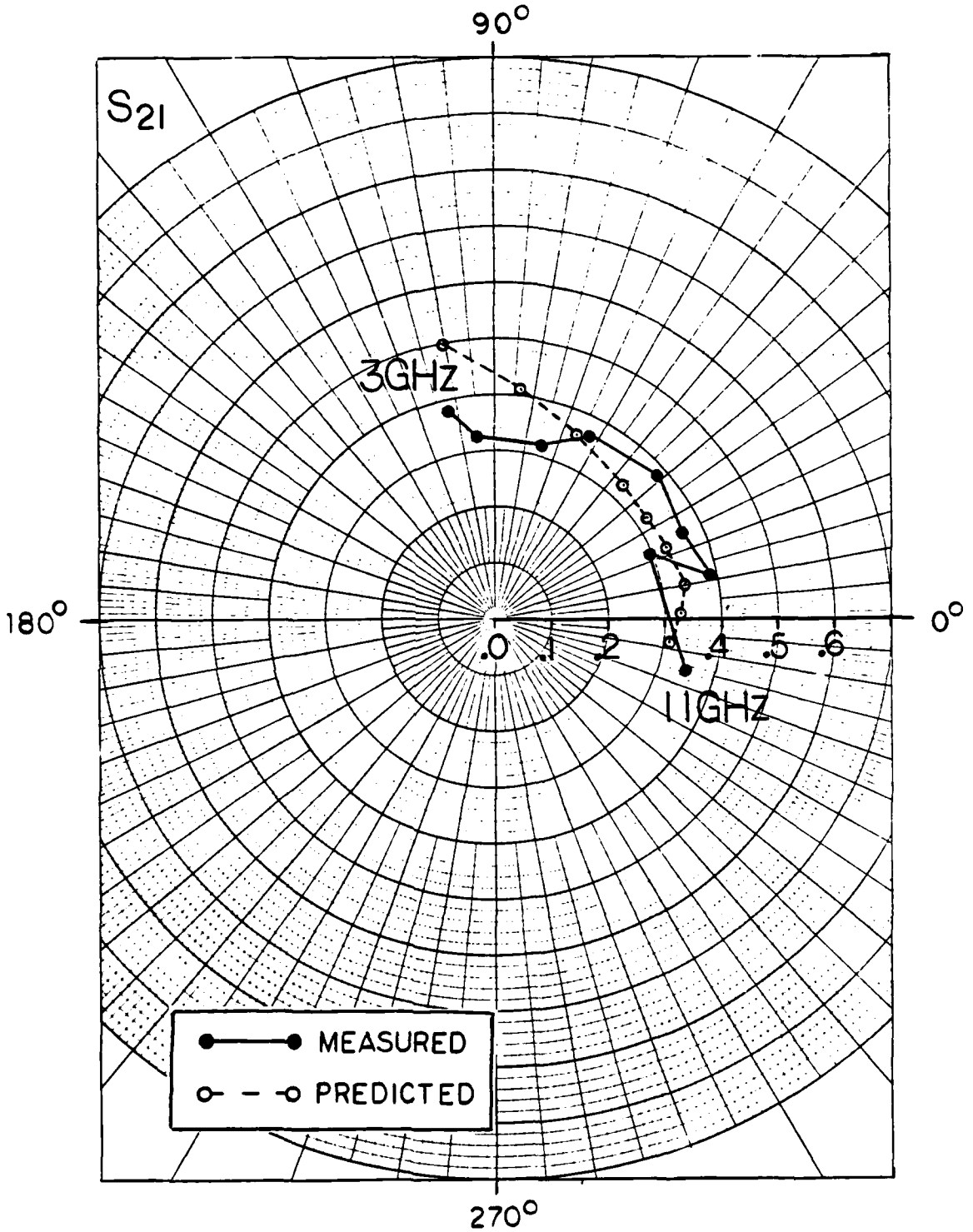


Figure 2.19 Predicted and measured S_{21} for the NE869177 MESFET. Bias: V_{DS} = 7.50 volts, V_{GS} = -6.00 volts.

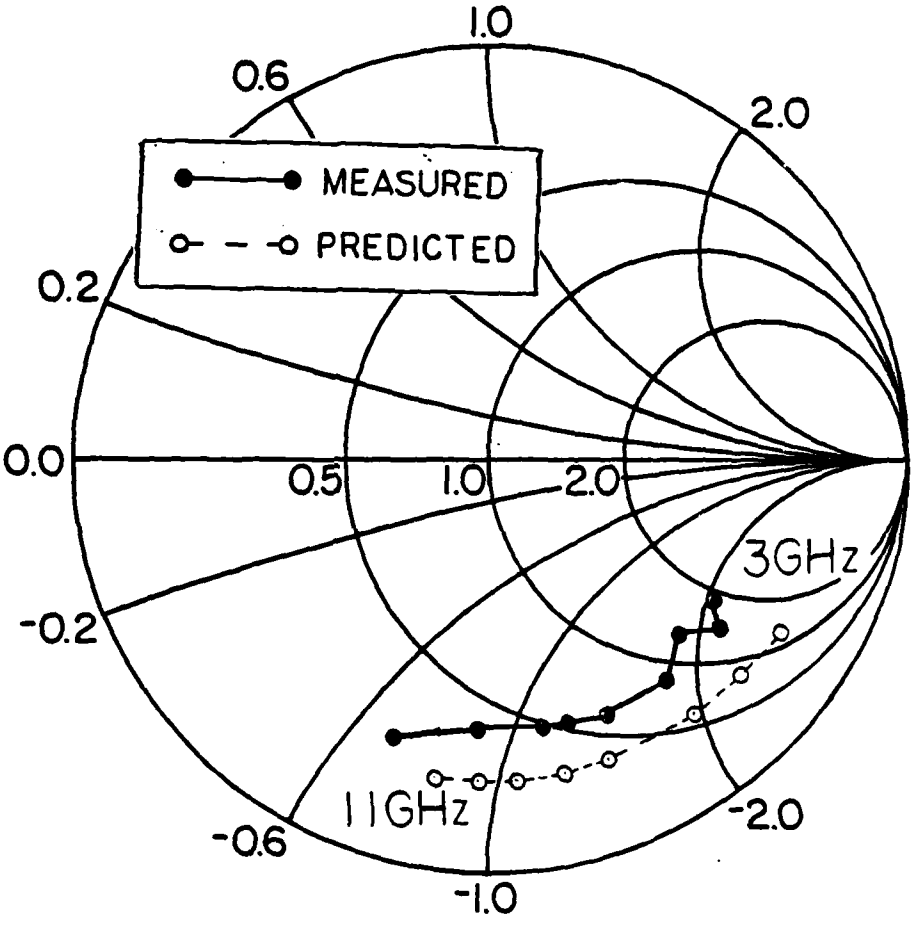


Figure 2.20 Predicted and measured S_{22} for the NE869177 MESFET. Bias: V_{DS} = 7.50 volts, V_{GS} = -6.00 volts.

LINEAR PARASITIC ELEMENT VALUES

R_S = 2.4 ohm

R_G = 8.0 ohm

R_D = 2.4 ohm

L_S = 0.025 nH

L_G = 0.100 nH

L_D = 0.100 nH

C_{GS} = 0.050 pF

C_{DS} = 0.050 pF

C_{GSC} = 0.500 pF

C_{DSC} = 0.010 pF

G_{SUBST} = 0.001 mho

Table 2.3 Parasitic element values for the NE869177 MESFET.

TEMPERATURE CORRECTED
BIAS SENSITIVE INCREMENTAL PARAMETERS

V_{DS} = 7.50V

	V_{GS} = -3.00V	V_{GS} = -6.00V
g_m	.060 mhos	.016 mhos
g_d	.001 mhos	.001 mhos
c_{11}	.473 pF	.423 pF
c_{12}	-.079 pF	-.079 pF
c_{21}	.00004 pF	.00004 pF
c_{22}	.243 pF	.239 pF
TRANSIT TIME	4.08 psec	3.69 psec
measured I_D	64.1 mA	4.4 mA
predicted I_D	64.3 mA	7.7 mA

Table 2.4 Incremental values for nonlinear elements from the basic MESFET model for the NE869177 MESFET.

2.3 LARGE-SIGNAL MODELING CONSIDERATIONS.

Figure 2.21 is an equivalent circuit for the nonlinear MESFET model and associated package parasitics. The linear parasitic elements were described in Section 2.2. The voltage controlled current source was investigated in Section 2.1, only here it is implemented with a voltage delay in the internal gate-source voltage to model transit time effects. The diodes model gate conduction current, which although strictly speaking is a static phenomenon, can be important under large-signal conditions.

The circuit of Figure 2.21 is suitable for large-signal time-domain circuit simulation using numerical integration such as presented in Chapter 3. An alternative representation will be developed in Chapter 4 for efficient large-signal frequency-domain circuit simulation.

2.3.1 Gate Conduction Current.

The gate of a MESFET is a Schottky barrier diode (9). It will conduct current when forward biased and also when reverse biased beyond a threshold voltage for avalanche breakdown. The forward conduction current characteristic is an exponential function of voltage, and

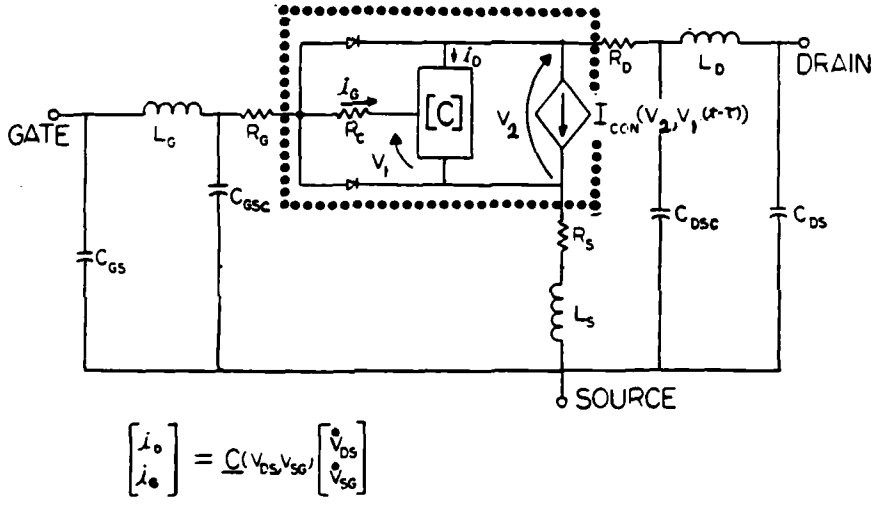


Figure 2.21 Packaged MESFET circuit for large-signal time-domain simulations.

the reverse current characteristic is superlinear but subexponential. Gate conduction current plays an insignificant role in static characteristics and small-signal S-parameters, because biasing the transistor to conduct such current would quickly result in the destruction of the delicate gate structure. However in large-signal microwave operation, the possibility exists that gate conduction can occur nondestructively over part of a period, and contribute to gain saturation and harmonic generation. This question has been raised by sampled waveform measurements conducted by Sechi, Huang, and Perlman (61).

Since gate conduction was not part of the Yamaguchi-Kodera model, it must be added externally to the Madjar-Rosenbaum basic nonlinear MESFET model by connecting gate-source and gate-drain diodes as indicated in Figure 2.21. The largest inherent error in such a procedure occurs at the onset of reverse breakdown, where appreciable current would simultaneously be carried by both the diode and the basic MESFET. There is less error for forward conduction, since the diode turn-on is more abrupt.

Detailed consideration of the nonlinear diode models will be deferred to the discussion of large-signal circuit simulations in Chapters 3 and 5. The frequency doubler simulations of Chapter 3 use a diode model with no reverse

breakdown. The overdriven amplifier experiments and simulations of Chapter 5 investigate both forward conduction and reverse breakdown.

2.3.2 An Upper Frequency Limit for the Lumped Element MESFET Model Approximation.

For the nonlinear lumped element MESFET model described in Section 1.4 to remain valid under large-signal conditions it is required that the drain conduction current and the incremental capacitances, determined by the charge distribution under the gate, be functions of the instantaneous values of the voltages V_1 and V_2. Under general large-signal conditions the drain current and capacitances will depend not only on the instantaneous values of V_1 and V_2, but also on their recent history. The determination of such a dependence requires the time dependent solution of Maxwell's equations in addition to the semiconductor equations under conditions imposed by the boundaries of the basic MESFET structure and the excitation from the external circuit. This would result in a distributed MESFET model.

Presently available MESFETs are not designed to be distributed devices. Gate lengths are fabricated as short as possible to achieve high gain-bandwidth products. A somewhat arbitrary upper frequency limit on the validity of the lumped element model approximation can be set by

requiring that a period of the applied signal voltage be greater than at least five electron transit times under the gate. Thus, a four picosecond transit time, such as calculated for the 0.5 micron gate NE869177 MESFET, would indicate an upper frequency limit of 50 GHz. The lumped approximation holds beyond the useful frequency range of the MESFET due to low-pass filtering effects of parasitic resistances and capacitances.

3. TIME-DOMAIN CIRCUIT SIMULATION

Once the physical nonlinear model is in hand, the next requirement for large-signal circuit design is to examine the device-circuit interactions. Perhaps the most obvious method for large-signal circuit simulation is the time-domain solution of the integrodifferential equations describing the circuit. When such equations are cast in normal form, that is with the first order time derivatives of the state variables expressed as functions of the state variables and time, standard numerical integration algorithms can be used to obtain the values of the state variables as functions of time. Initial values for the state variables must be assigned at the start of integration, and if it is desired to obtain a steady-state solution, integration must proceed over several periods until the transient response resulting from the initial guess has died out. This is the case in the analysis that is presented here. Once steady-state has been achieved, the state variables for a final period can be examined directly as waveforms, or can be processed through a discrete Fourier transform (62) to obtain a frequency-domain representation of the currents and voltages of interest. The entire procedure is diagramed in Figure 3.1. This Chapter will

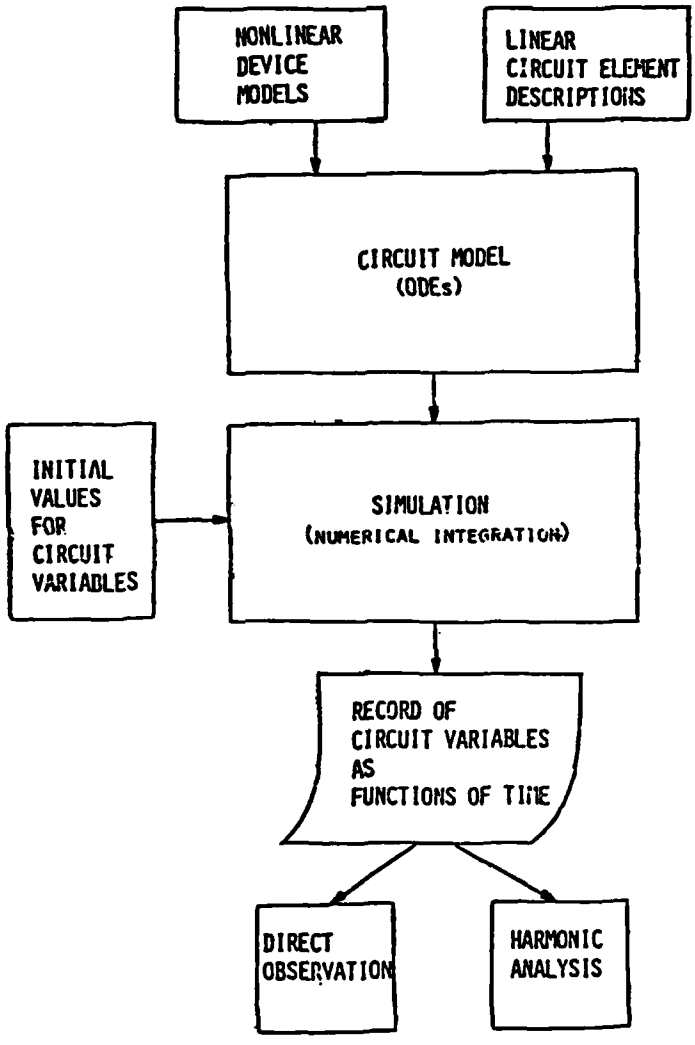


Figure 3.1 Time-domain large-signal circuit simulation procedure using numerical integration of the ordinary differential equations modelling the circuit.

present the use of the nonlinear MESFET model in a microwave frequency doubler circuit simulation.

3.1 NUMERICAL INTEGRATION ALGORITHM

A fourth order Runge-Kutta algorithm (63) was originally used with the Madjar-Rosenbaum large-signal MESFET model for overdriven amplifier simulations conducted by Green and Rosenbaum (64). On the basis of this experience, it was decided to adopt a multistep predictor-corrector algorithm for improvement in computational efficiency. The program that was adopted was C. W. Gear's DIFSUB (65), which allows the user to choose between an Adams-Bashforth predictor - Adams-Moulton corrector, or Gear's stiffly stable algorithm. Gear's stiffly stable algorithm was created to handle stiff systems of ordinary differential equations, that is systems where the eigenvalues of the associated Jacobian differ by more than an order of magnitude. In the present context, this would indicate circuit simulations with frequency components differing by more than a factor of ten.

Both DIFSUB options were investigated using stiff and nonstiff systems of test equations for speed of execution and accumulated error. Automatic step size and integration order features were also examined. Figure 3.2

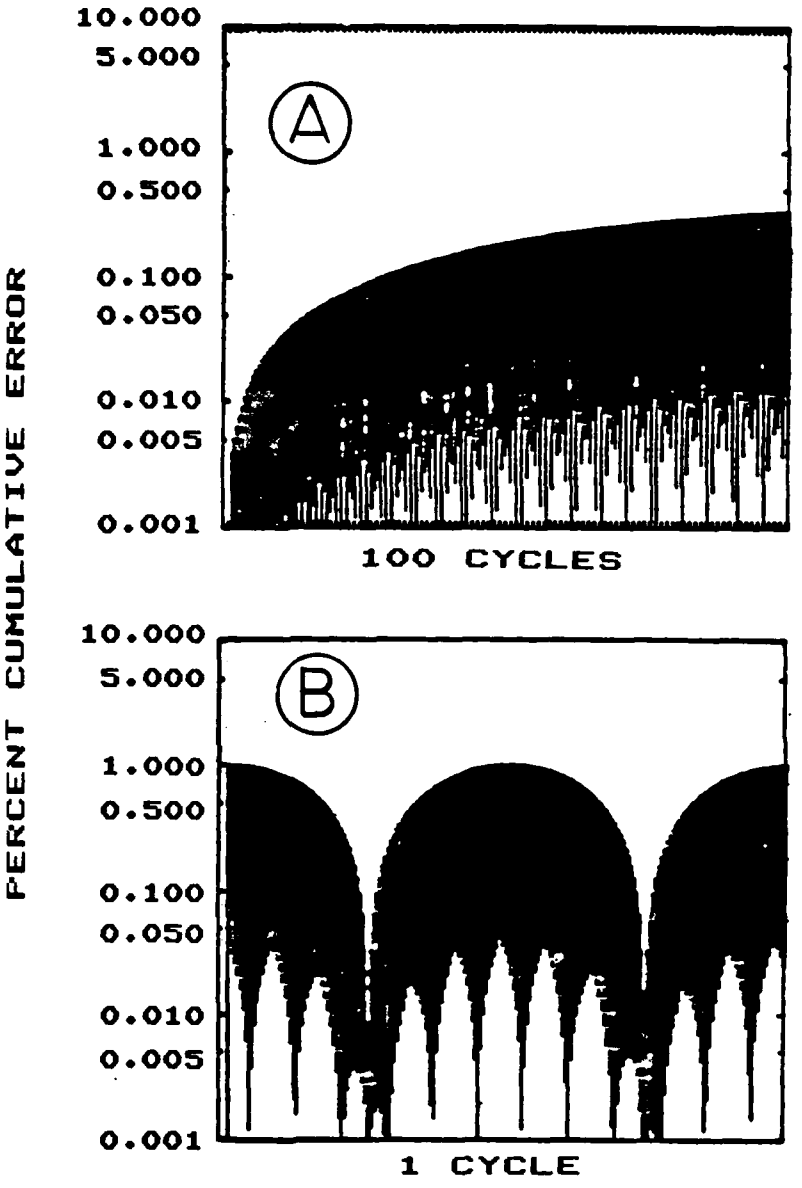


Figure 3.2 Accumulated error plots for the Adams-Bashforth-Moulton numerical integration algorithm: Figure 3.2A - nonstiff, Figure 3.2B - stiff.

contains accumulated error plots for the nonstiff test (Figure 3.2A) and the stiff test (Figure 3.2B). The test equations for Figure 3.2A were:

$$\frac{dY_1}{dt} = - Y_2$$

$$\frac{dY_2}{dt} = Y_1$$

with initial conditions:

$$Y_1(0) = 1$$

$$Y_2(0) = 0$$

The solution is:

$$Y_1 = \cos(t)$$

$$Y_2 = \sin(t)$$

Figure 3.2A is a plot of the difference between the numerical and analytic solution values for Y1 as a function of time for 100 cycles. It was found that the accumulated error remained bounded for the Adams-Bashforth-Moulton option when the maximum order was fixed at two, and the maximum error allowed per integration step was set at less than 0.5 percent.

Figure 3.2B is a similar plot, but for a set of test equations which generated a cosine amplitude modulated

cosine wave. This was a stiff system because the ratio of the carrier frequency to the modulation frequency was 100:1. The result is plotted for one modulation period. Even for the stiff case, the Adams-Bashforth-Moulton algorithm was more efficient than Gear's algorithm. As a result of these tests, it was decided to use the Adams algorithm for the frequency doubler simulations discussed in Section 3.3.

3.2 LOOKUP TABLE STORAGE OF MESFET MODEL RESULTS

As observed in Section 1.4, the output from the Madjar-Rosenbaum basic nonlinear MESFET model, for a specific transistor, can be viewed as a collection of five surfaces (Figures 1.5 and 1.6). Because time-domain large-signal circuit simulations may require tens of thousands of calls to the nonlinear MESFET model, it is much more efficient to use it to generate five such surfaces for a particular transistor, and store the surfaces in a table as functions of V_1 and V_2. A computer program has been created which does this, and reads and linearly interpolates results from the table as required during numerical integration. This procedure was used for the simulations described in the next section. One lookup table containing MESFET model output values corresponding to over two thousand V1,V2 pairs was created for the 1.7

micron gate length MESFET described in Table 2.1. The FET temperature assumed for these calculations was 300 K. The execution time on a PDP 11/45 minicomputer with overlayed program structure was about two hours.

Since the Madjar-Rosenbaum MESFET model will not operate with negative values of V_2 (internal drain-source voltage), only positive V_2 is used in generating the lookup table. To accommodate the possibility that V_2 may become negative during large-signal simulations, additional software was written to reverse the model as it is read from the table by interchanging source and drain, and transforming the voltage reference node to the drain.

A more economical lookup table generation approach has been created which uses a combination of linear interpolation and specifically devised curve fitting, determined by the functional forms of the MESFET model output (Figures 1.5 and 1.6) - which yields results of comparable quality. This was motivated by the need to generate many tables for the same transistor at different operating temperatures. Using this new approach, table generation typically requires fewer than one hundred calls to the basic MESFET model.

The common-source drain current characteristics (Figure 1.5) are linear functions of V_2, the internal drain-source voltage, for values of V_2 above the onset of current saturation. Below saturation, the characteristics

are parabolic, reflecting the approximation for the V(E) curve (Figure 2.4B) used in deriving the nonlinear model. (The piecewise-linear V(E) approximation shown in Figure 2.4A resulted in piecewise-linear drain current I-V characteristics.) Consequently, the characteristics for a given value of V_1, the internal gate-source voltage, can be adequately reproduced from four parameters obtained from the MESFET model: (i.) the value of g_D at V_2=0, g_{DO}; (ii.) the value of V_2 at which the drain current saturates, V_{2SAT}; (iii.) the value of the drain current at the onset of saturation, I_{DSAT}; and (iv.) the value of g_D in drain current saturation, g_{DSAT}. The table generation program obtains these parameters for ten values of V_1, ranging from the built-in potential of the Schottky barrier gate to the cut-off voltage. When the table is read during the course of a large-signal circuit simulation, the values of the four parameters are linearly interpolated as functions of V_1, and the drain current is calculated for values of V_2 less than V_{2SAT} using:

$$I_D(V_1,V_2) = I_{DSAT}(V_1) - \frac{g_{DO}^2(V_1)}{4I_{DSAT}(V_1)} [V_2 - V_{2SAT}(V_1)]^2 ,$$

and for values of V2 greater than or equal to V2SAT using:

$$I_D(V_1,V_2) = I_{DSAT}(V_1) + g_{DSAT}(V_1) [V_2 - V_{2SAT}(V_1)] .$$

The incremental capacitances are similarly calculated as functions of V_1 and V_2, with the necessary parameters being obtained from the MESFET model at the same time as the drain conduction current parameters are obtained, requiring few additional calls to the model. C_{11}, C_{12}, and C_{21} are expressed as parabolic functions of V_1 and V_2. C_{22} is parabolic with respect to V_1, and is linearly interpolated with respect to V_2. The accuracy of these approximations is in keeping with the precision of the basic MESFET model. This newer version of the lookup table was used for the frequency-domain simulations which will be discussed in Chapter 5.

3.3 SIX TO TWELVE GHz FREQUENCY DOUBLER SIMULATIONS

The MESFET used for these simulations is the 1.7 micron gate-length transistor described in Table 2.1. The circuit model for the transistor, including package parasitics, is displayed in Figure 2.21. The gate conduction current diode models are peicewise linear, with zero conductance until the forward turn-on voltage of of 0.7 Volts is reached, at which point the resistance drops to zero. The FET frequency doubler circuit is snown in Figure 3.3. The input power at 6 GHz is derived from the sinusoidal voltage source in series with R_{GN}. Output power is delivered to R_L. R_{GN} and R_L were chosen to be

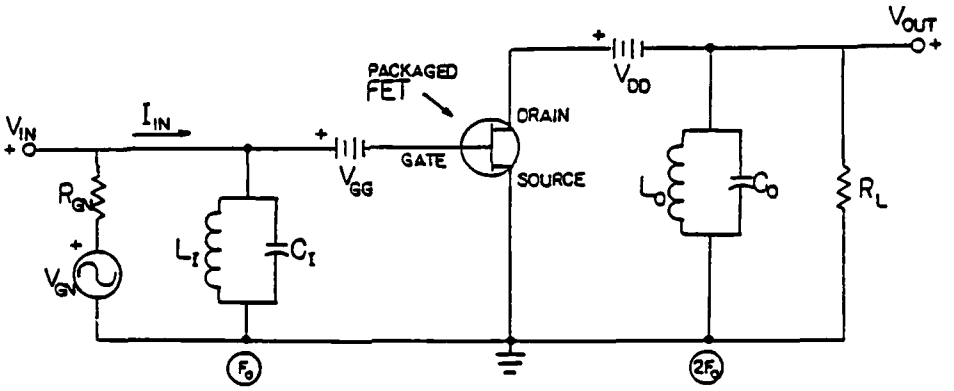


Figure 3.3 Circuit for initial MESFET frequency doubler simulations. ($R_{GN} = R_L = 200$ ohms.)

200 ohms in order to minimize the loading of the input and output tuned circuits, while at the same time being reasonable to construct in an eventual prototype. These values could be realized with quarter-wave transformers terminated in 50 ohms.

L_I and C_I were initially chosen with cautious guidance from the calculated small-signal scattering parameters of the packaged FET model. Circuit simulations were then performed over a range of L_I values for the purpose of tuning to improve performance. Figure 3.4 displays 6-12 GHz doubler gain as a function of L_I. The "doubler gain" is the ratio of the second harmonic power delivered to RL to the fundamental power available from the generator (P1 available). Figure 3.5 shows the voltage standing wave ratio on the line between the generator and the input tuned circuit. Minimum VSWR and maximum doubler gain do not occur at the same value of L_I. This indicates that input matching does not necessarily result in input current and voltage waveforms for the best doubler performance.

Similarly L_O and C_O were chosen for output resonance at 12 GHz, and L_O was subsequently experimentally "tuned" to maximize doubler gain (Figure 3.6). Figure 3.7 shows output spectral purity as a function of L_O. Spectral purity is defined as the ratio of second harmonic power delivered to RL to the total r.f. power delivered to R_L.

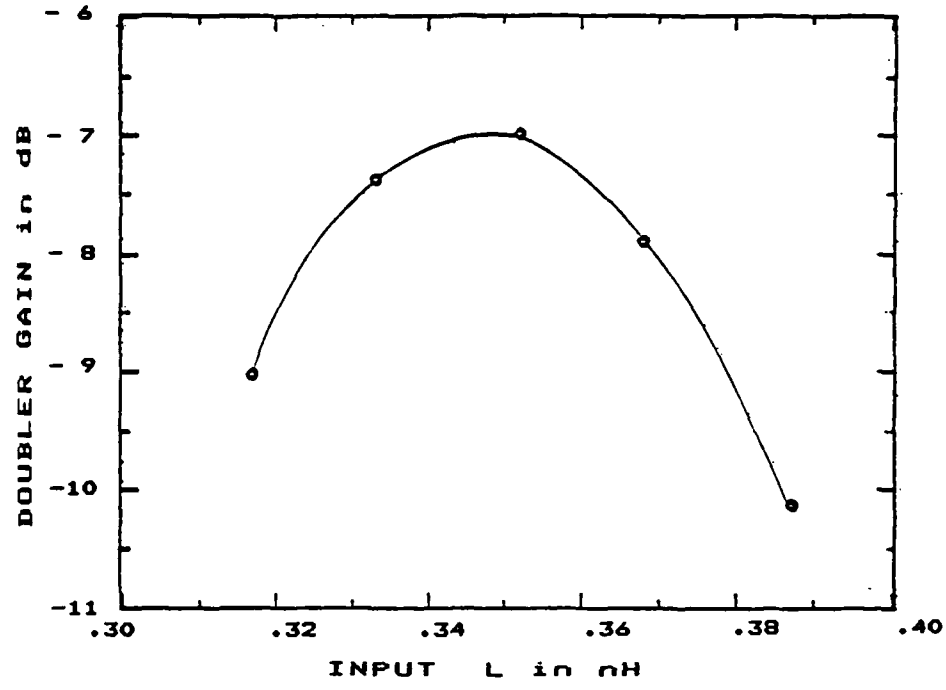


Figure 3.4 6-12 GHz doubler gain as a function of L_I. Fixed conditions:

C_I = 1.475 pF,
L_0 = 0.176 nH,
C_0 = 0.769 pF,
V_{DD} = 6.0V,
V_{GG} = 4.0V,
P_1 available = 12.66 mW.

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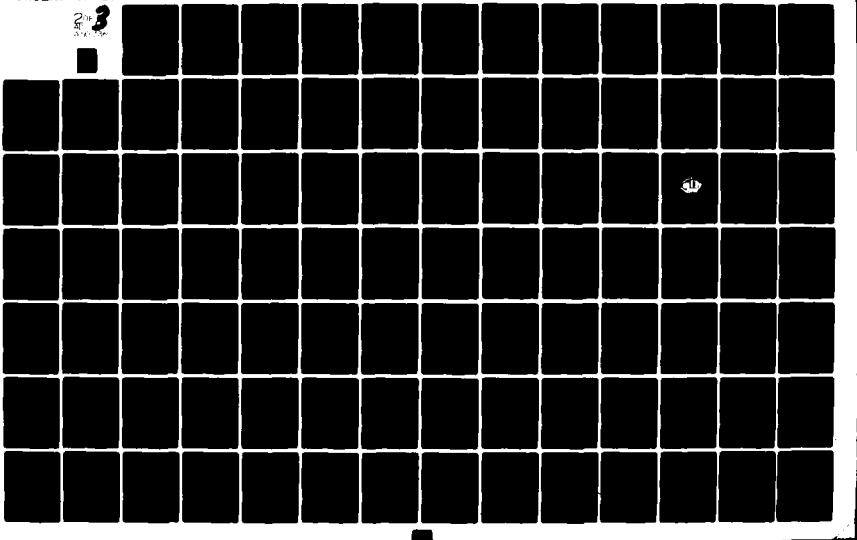


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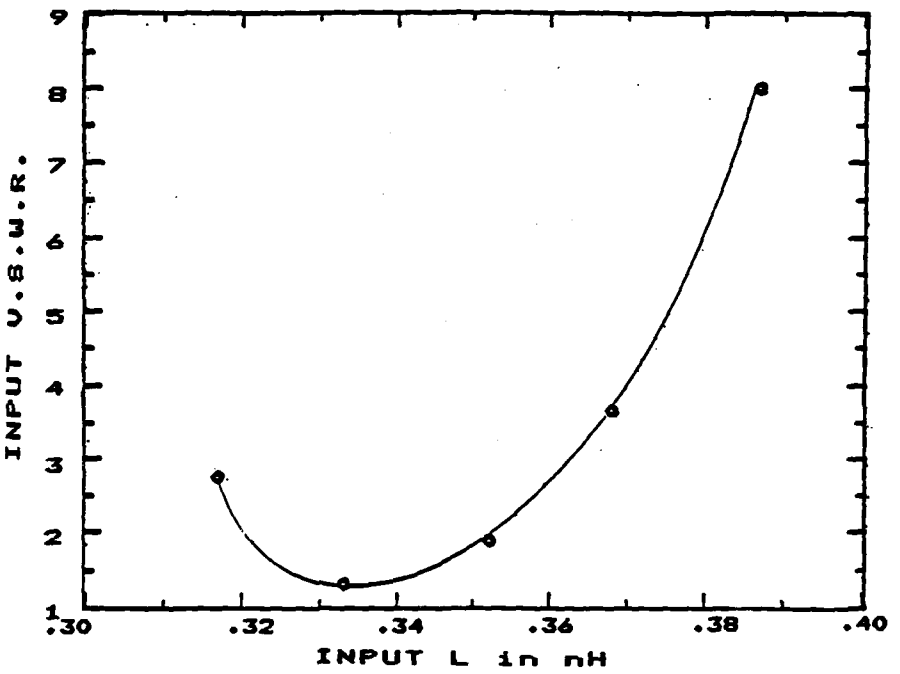

Figure 3.5 6-12 GHz doubler input voltage standing wave ratio as a function of L_I. (Same fixed conditions as in Figure 3.4.)

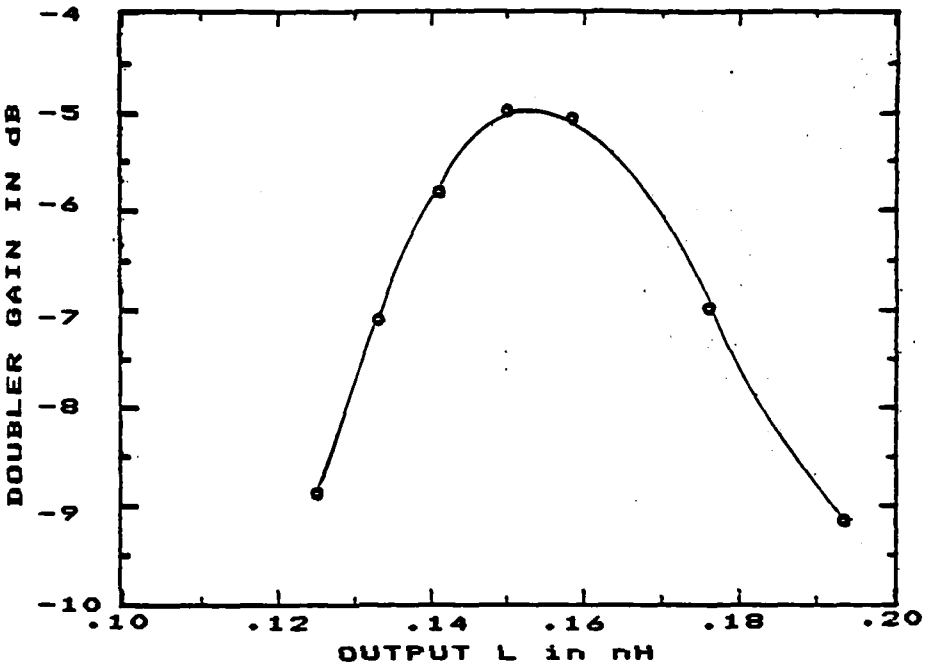

Figure 3.6 6-12 GHz doubler gain as a function of L_0. Fixed conditions:

L_I = 0.352 nH,
C_I = 1.475 pF,
C_0 = 0.769 pF,
V_{DD} = 6.0V,
V_{GG} = 4.0V,
P_1 available = 12.66 mW.

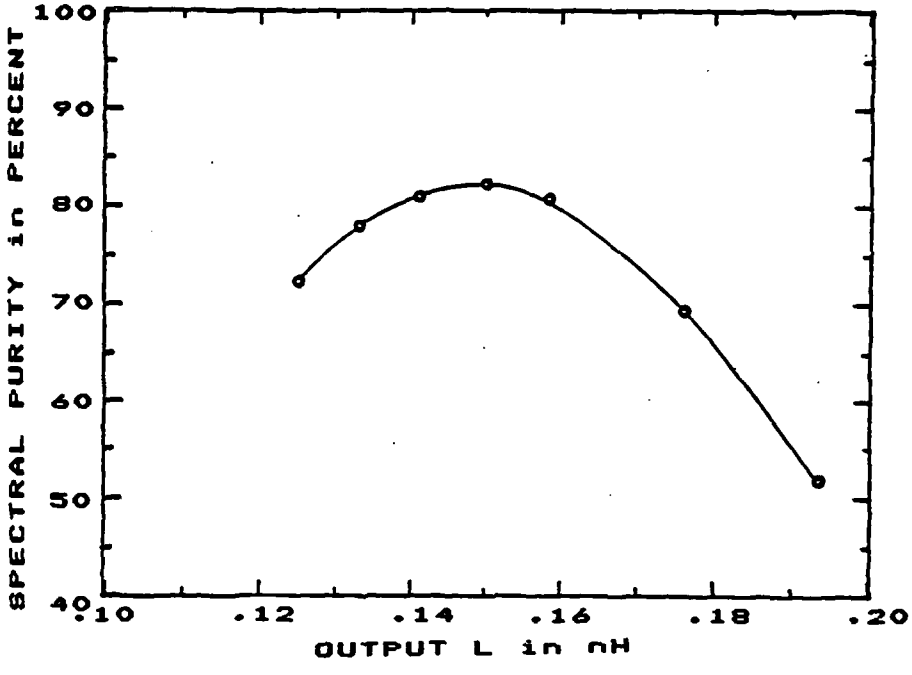

Figure 3.7 6-12 GHz doubler, output spectral purity as a function of L_0. (Same fixed conditions as in Figure 3.6.)

The maxima in Figures 3.6 and 3.7 occur at about the same value of L_O, so there is no need to make spectral purity - doubler gain trade-offs in output tuning. Adjustment of L_O and R_L (not shown) to effect a conjugate impedance match of the parallel L_O, C_O, and R_L combination to S_{22} of the packaged FET at 12 GHz resulted in a 23 dB loss in doubler gain when compared to a simulation using empirically selected "best tuning". This reinforces the sense of caution that must be exercised in applying linear system concepts to nonlinear systems.

Figures 3.8 through 3.10 present results of a series of simulations in which the power available from the 6 GHz generator was varied. Doubler gain, input VSWR, and output spectral purity all increase monotonically with P_1 available over the range that was investigated. Spectral purity saturates sooner than doubler gain.

Figures 3.11 and 3.12 show doubler gain and output spectral purity as functions of drain bias, V_{DD}. In Figure 3.11, there is a rather sharp doubler gain maximum near V_{DD} = 10 V. Maximum output spectral purity is also observed at this V_{DD} value. Input VSWR was found to be relatively insensitive to V_{DD}.

The effect of gate bias, V_{GG}, is examined in Figures 3.13, 3.14 and 3.15. The doubler gain curve has a characteristic double hump appearance. The humps would probably appear somewhat more symmetric if the input

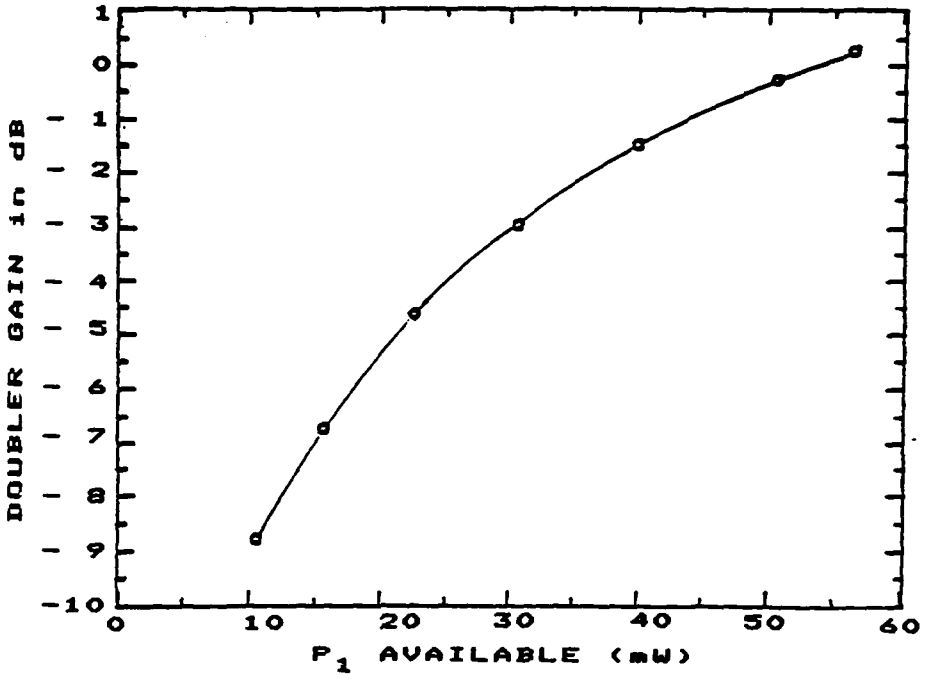

Figure 3.8 6-12 GHz doubler gain as a function of power available from the 6 GHz generator. Fixed conditions:

L_I = 0.352 nH,
C_I = 1.475 pF,
L_0 = 0.158 nH,
C_0 = 0.769 pF,
V_{DD} = 10.0 V,
V_{GG} = 4.0 V.

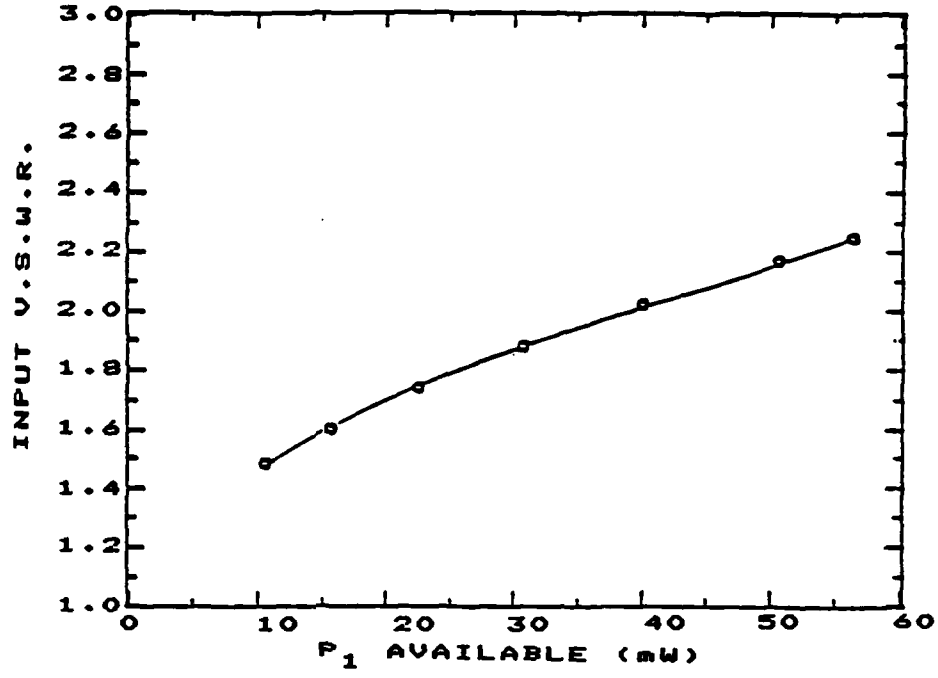

Figure 3.9 6-12 GHz doubler, input voltage standing wave ratio as a function of power available from the 6 GHz generator. (Same fixed conditions as in Figure 3.8.)

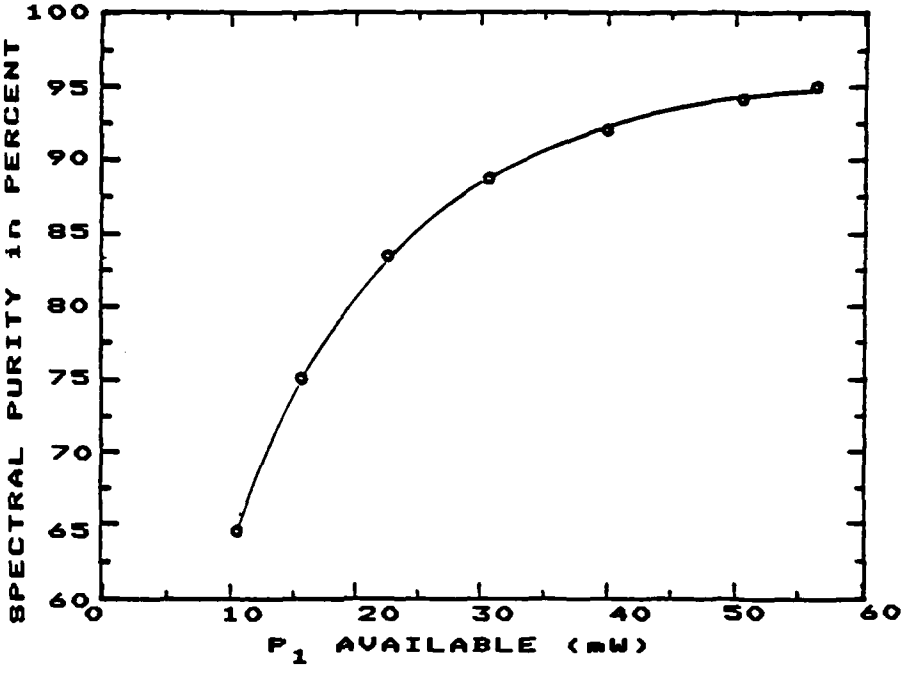

Figure 3.10 6-12 GHz doubler, output spectral purity as a function of power available from the 6 GHz generator. (Same fixed conditions as in Figure 3.8.)

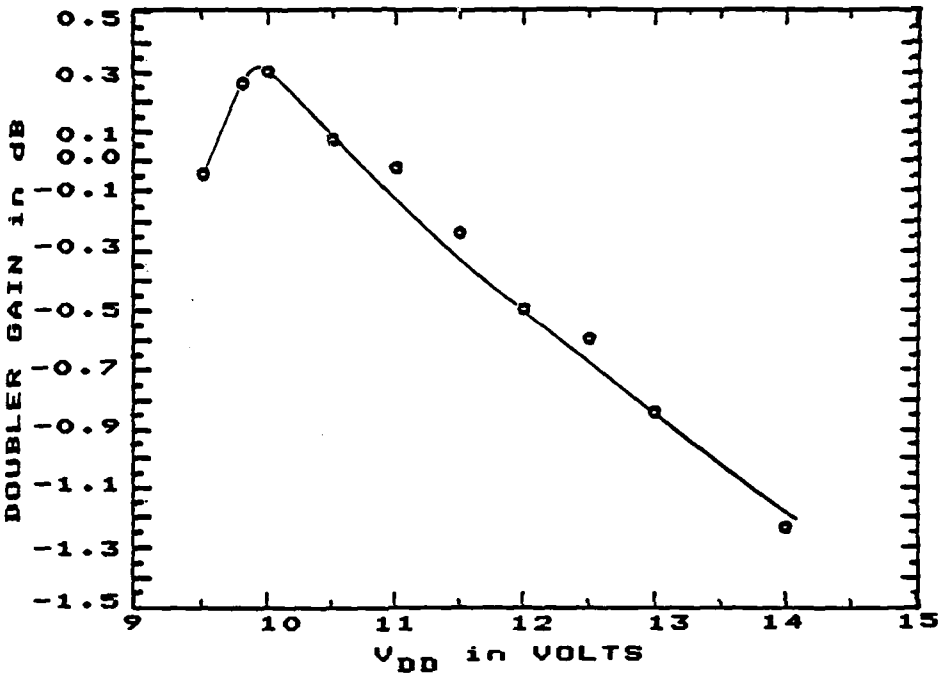

Figure 3.11 6-12 GHz doubler gain as a function of V_{DD}. Fixed conditions:

L_I = 0.352 nH,
C_I = 1.475 pF,
L_0 = 0.158 nH,
C_0 = 0.769 pF,
V_{GG} = 4.0 V,
P_1 available = 56.41 mW.

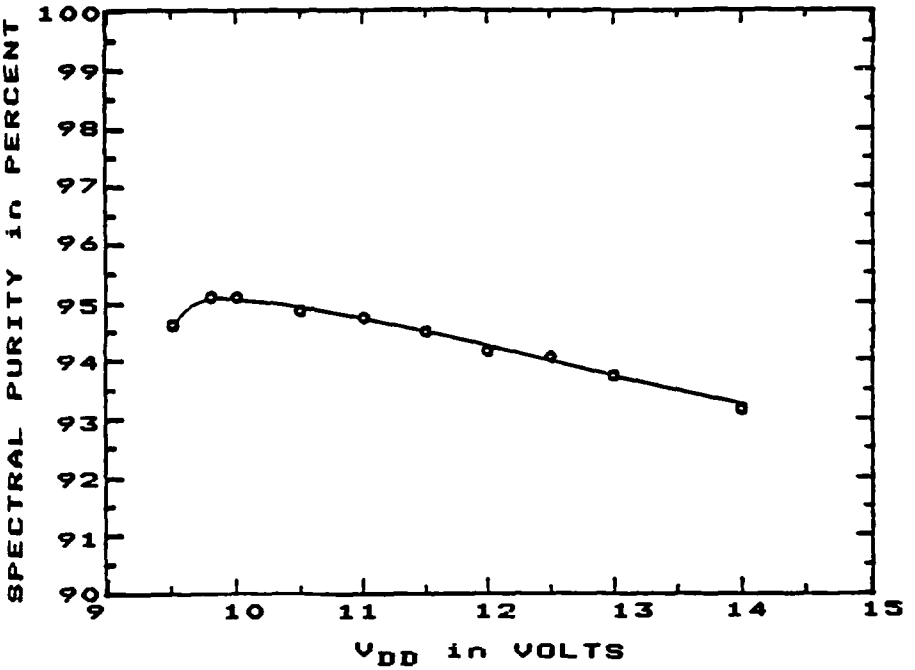

Figure 3.12 6-12 GHz doubler, output spectral purity as a function of V_{DD}. (Same fixed conditions as in Figure 3.11.)

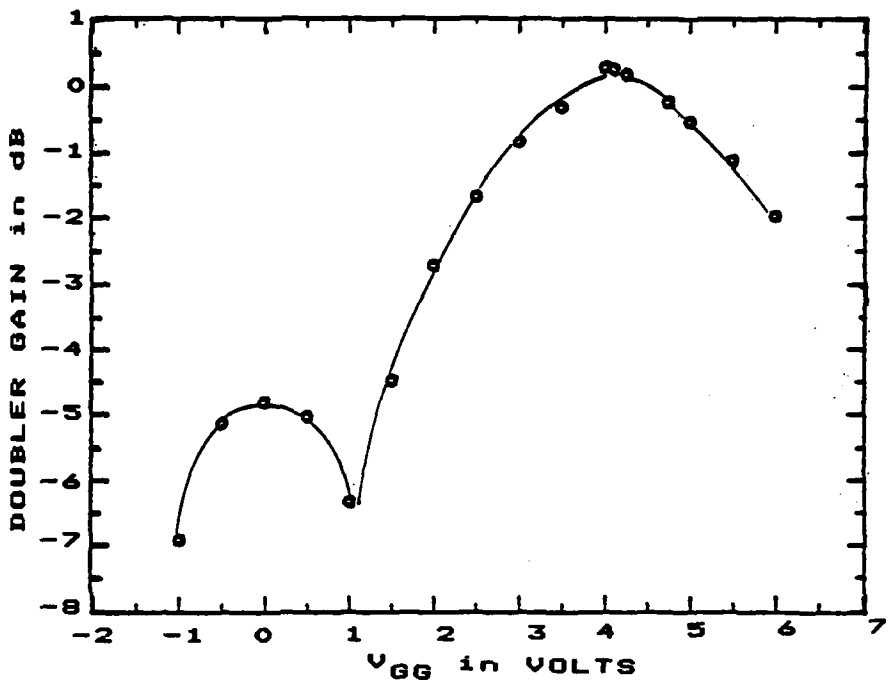

Figure 3.13 6-12 GHz doubler gain as a function of V_{GG}. Fixed conditions:

L_I = 0.352 nH,
C_I = 1.475 pF,
L_0 = 0.158 nH,
C_0 = 0.769 pF,
V_{DD} = 10.0 V,
P_1 available = 56.41 mW.

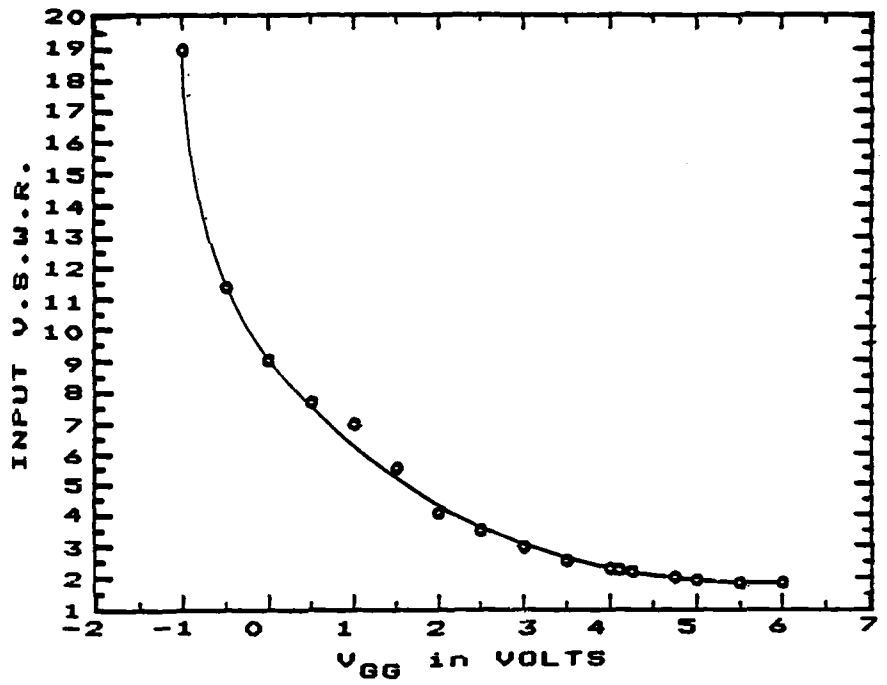

Figure 3.14 6-12 GHz doubler, input voltage standing wave ratio as a function of V_{GG}. (Same fixed conditions as in Figure 3.13.)

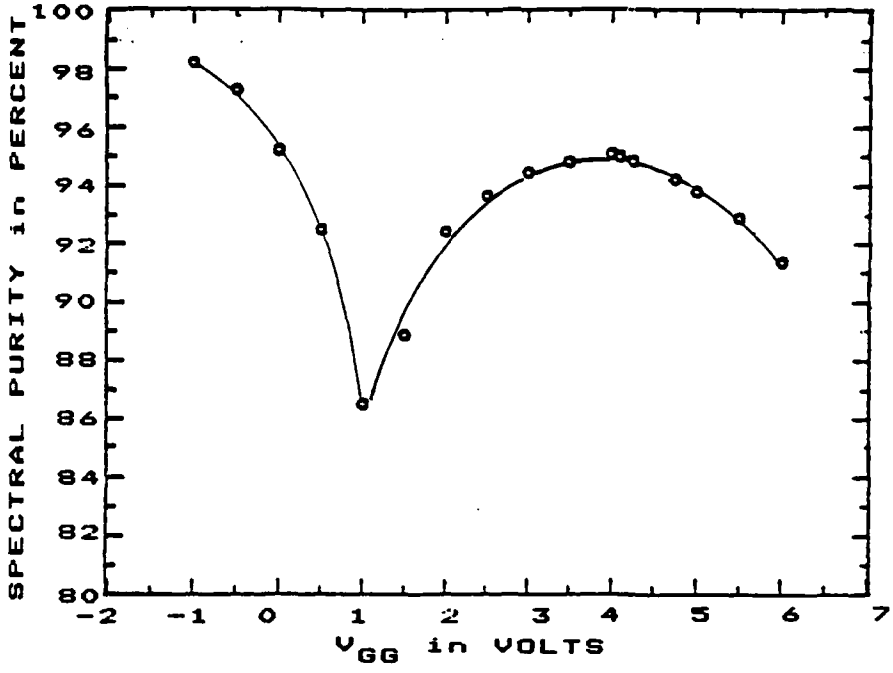

Figure 3.15 6-12 GHz doubler, output spectral purity as a function of V_{GG}. (Same fixed conditions as in Figure 3.13.)

tuning had also been adjusted to maximize doubler gain at each V_{GG} value. Input VSWR increases dramatically as V_{GG} becomes negative. The more negative it becomes, the greater the chance of gate conduction occurring during part of each period and effectively shorting the doubler's input. The output spectral purity curve resembles the product of the doubler gain and input VSWR curves. By taking such a product, one would essentially be redefining doubler gain as the ratio of second harmonic output power to fundamental input power (rather than available fundamental input power).

Figures 3.16 through 3.21 are waveforms and state space trajectories from the the 6-12 GHz doubler simulation which had the best doubler gain. Figures 3.16 and 3.17 are input voltage and current waveforms for one 6 GHz period. Figure 3.18 is the corresponding current-voltage trajectory. Examination of Figure 3.18 reveals that steady-state operation has nearly been achieved, since the limit cycle is nearly closed. It is also evident that for part of the cycle, there is a substantial reactive component to the load that the doubler circuit presents to the generator. Figure 3.19 is the voltage waveform across the output load resistor, R_L. Frequency doubling is obvious in the Lissajous figure pesented in Figure 3.20, the output voltage-input voltage trajectory. Some first harmonic content in the output

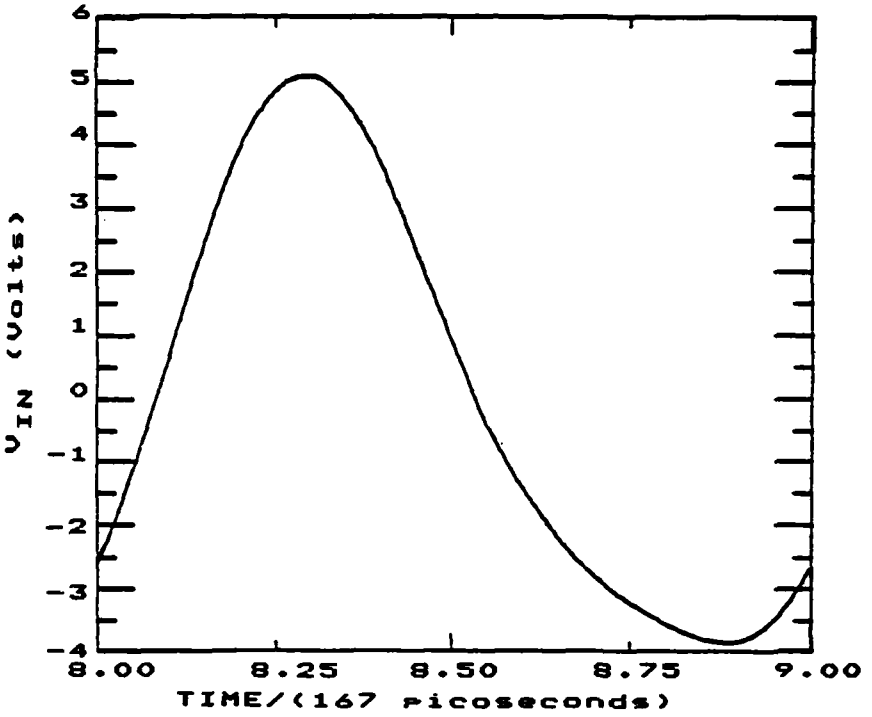

Figure 3.16 6-12 GHz doubler, input voltage waveform for 9th period.

L_I = 0.352 nH
C_I = 1.475 pF
L_0 = 0.158 nH
C_0 = 0.769 pF
V_{DD} = 10.0 V
V_{GG} = 4.0 V

P_1 available = 56.41 mW

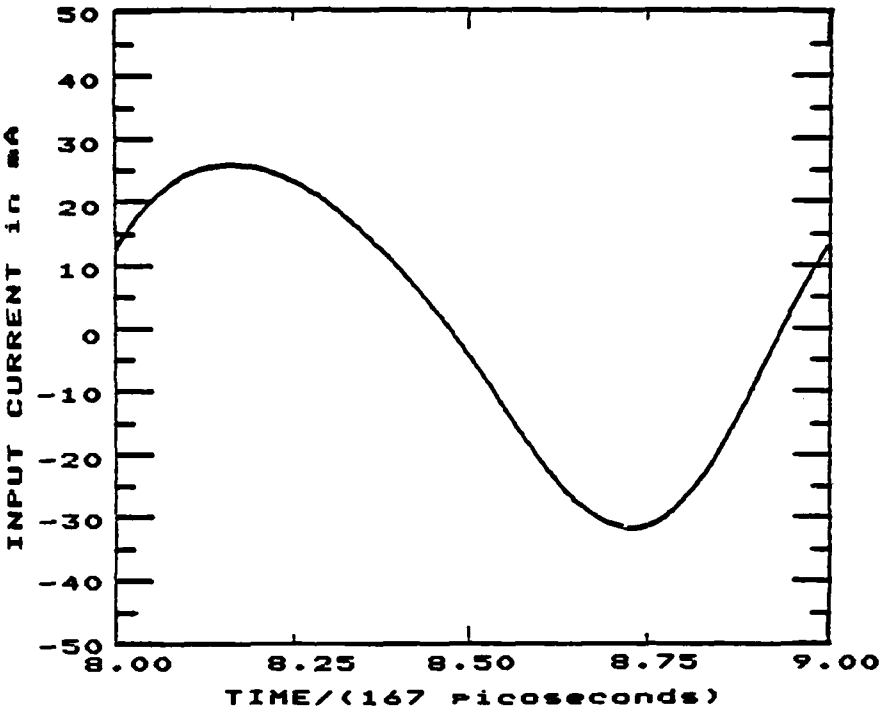

Figure 3.17 6-12 GHz doubler, input current waveform for 9th period. (Same simulation as in Figure 3.16.)

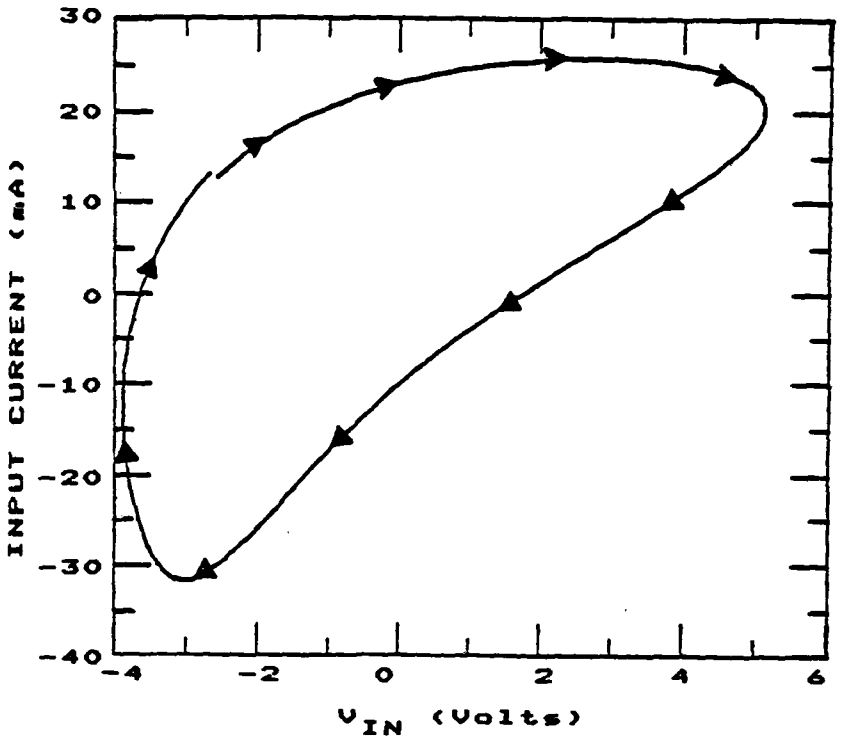

Figure 3.18 6-12 GHz doubler, input current-input voltage trajectory for 9th period. (Same simulation as in Figure 3.16.)

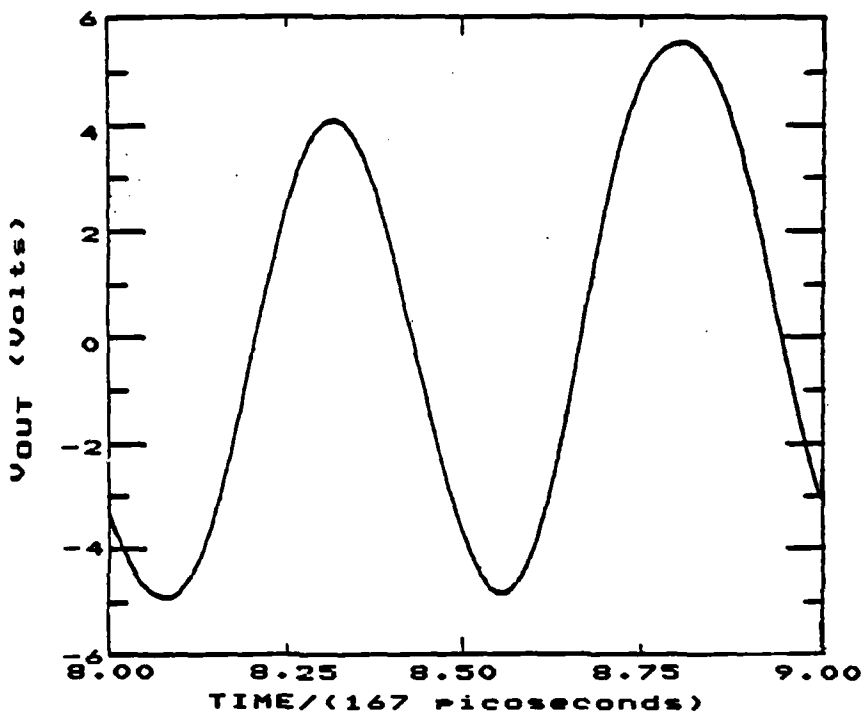

Figure 3.19 6-12 GHz doubler, output voltage waveform for 9th period. (Same simulation as in Figure 3.16.)

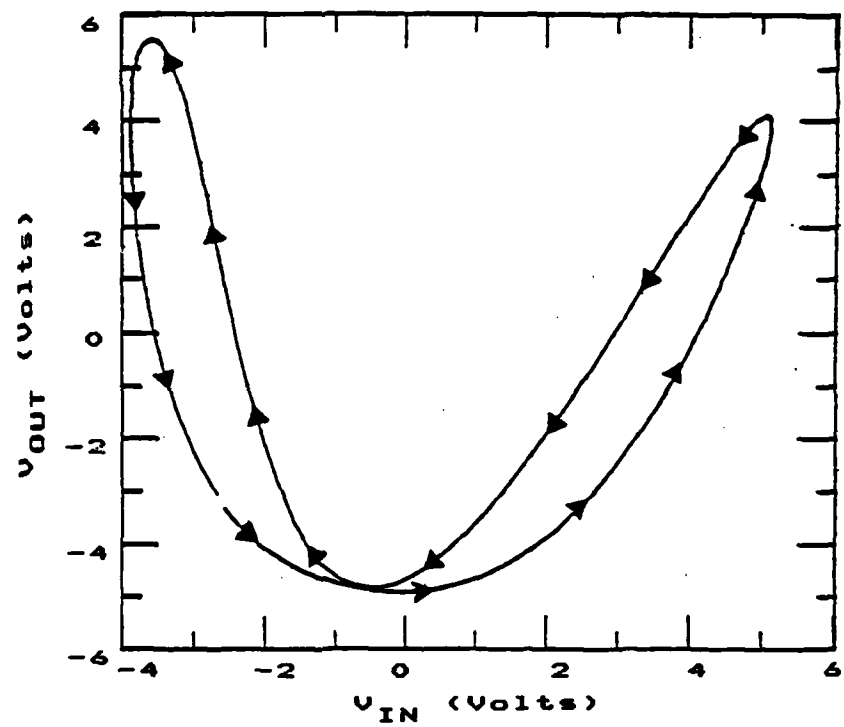

Figure 3.20 6-12 GHz doubler, output voltage-input voltage trajectory for 9th period. (Same simulation as in Figure 3.16.)

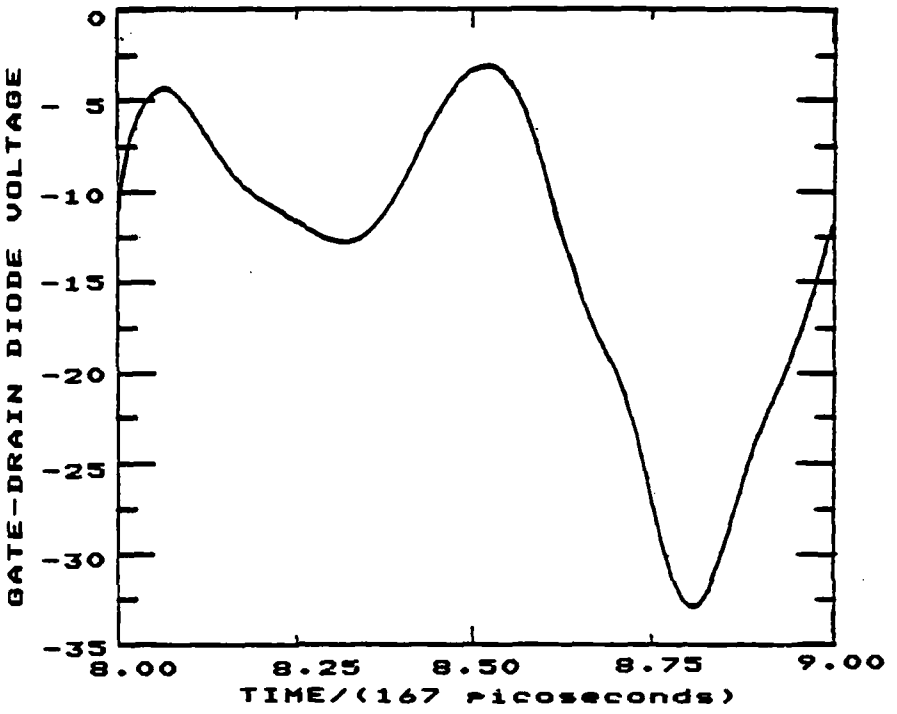

Figure 3.21 6-12 GHz doubler, gate-drain voltage waveform for 9th period. (Same simulation as in Figure 3.16.)

voltage is also apparent from the slight assymetry. The second harmonic (12 GHz) power delivered to R_L is 60.5 mW, while the first harmonic (6 GHz) power delivered to R_L is 2.9 mW. Figure 3.21, the voltage waveform across the gate to drain diode of Figure 2.21, shows a -33 V minimum, which raises the issue of including reverse breakdown behavior in the gate conduction diode models. This will be considered in Chapter 5. For this simulation, the doubler gain was 0.31 dB, the input VSWR was 2.25, and the output spectral purity was 95.1%.

Gupta, Laton and Lee (66) have performed actual doubler experiments using a very similar circuit. Their results for doubler gain as a function of V_{GG} is shown in Figure 3.22 for various values of V_{DD} for a 4-8 GHz MESFET doubler. When compared with Figures 3.11 and 3.13 it is seen that there is qualitative agreement, with the double hump structure as a function of V_{GG} evident in both simulated and measured results. Although the results cannot be strictly compared because of transistor, circuit, and frequency differences in the simulations and measurements, the work presented in this chapter does demonstrate the use of the nonlinear MESFET model in understanding large-signal circuit operation, using time-domain simulation.

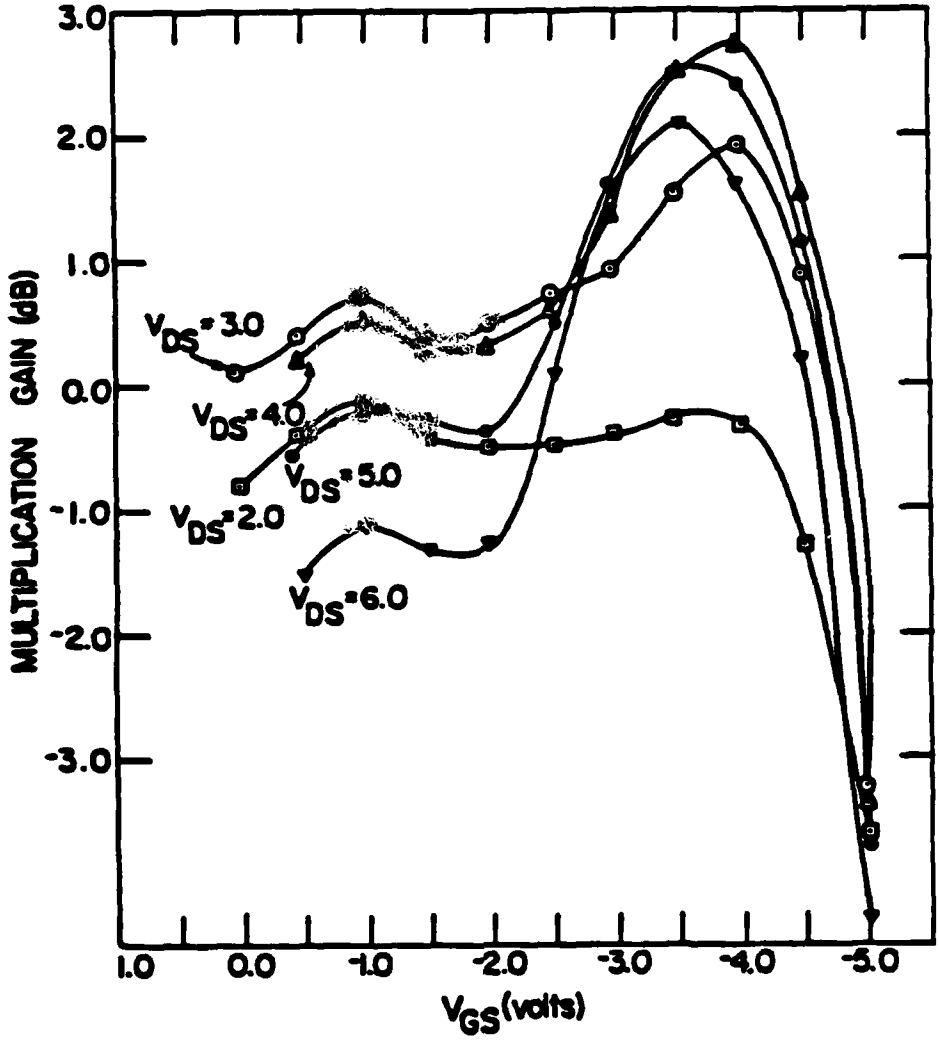

Figure 3.22 Experimental results for MESFET frequency doubler gain as a function of gate-source voltage, with drain-source voltage as a parameter. (After Gupta, Laton, and Lee, "Performance and Design of Microwave FET Harmonic Generators," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-29, No. 3, March 1981, page 262.)

4. FREQUENCY-DOMAIN CIRCUIT SIMULATION

The disadvantages of time-domain nonlinear circuit simulation using numerical integraton include: long computation timé to obtain steady-state results, problems with handling large or distributed linear subnetworks, and difficulty in handling the time constants associated with realistic biasing networks. For the determination of steady-state responses for nonlinear circuits, frequency-domain simulation approaches are preferable not only because of potential improvements in computational efficiency, but also because they permit the direct use of frequency domain descriptions of linear subnetworks. This chapter presents a frequency-domain circuit simulation technique that was developed for use with the nonlinear MESFET model which was presented earlier. The usefulness of this technique is demonstrated in the overdriven MESFET amplifier simulations of Section 5.2

4.1 STEADY-STATE SIMULATION ALGORITHM

The MESFET circuit is partitioned as shown in Figure 4.1. The network to the left of the linear-nonlinear interface is entirely linear. The nonlinear MESFET model is to the right. Since a steady-state solution is sought,

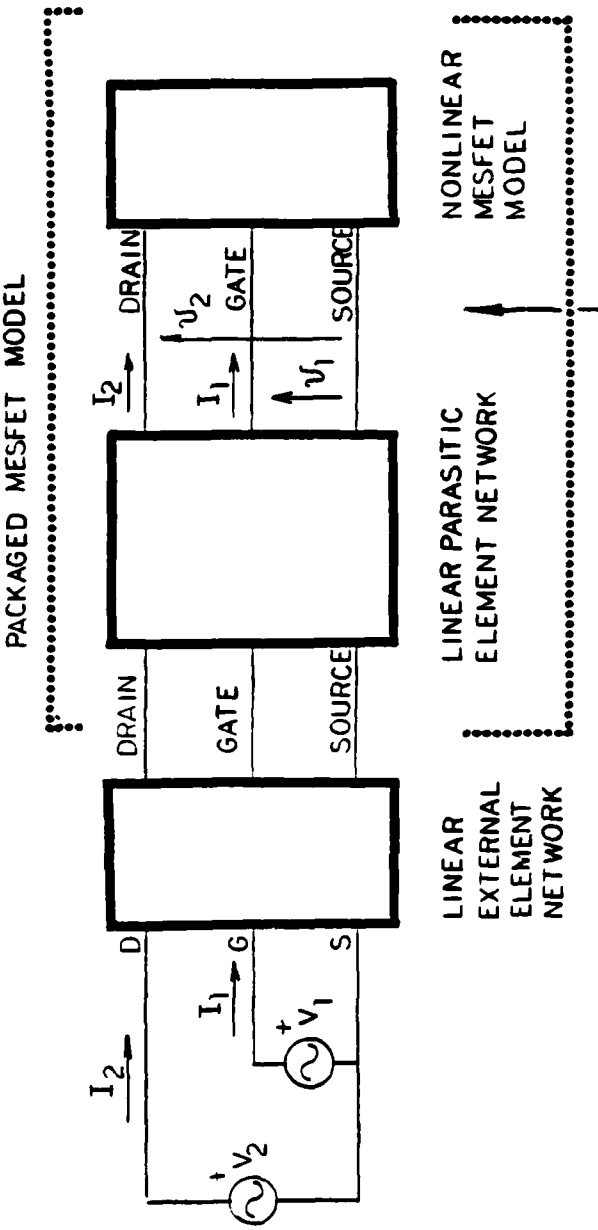

Figure 4.1. Partitioning of the MESFET circuit for frequency-domain simulations.

knowledge that the currents and voltages are periodic with a fundamental radian frequency of ω, permits their representation as Fourier series:

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \sum_{n=0}^{N} \left\{ \begin{bmatrix} v_{1,n}^R \\ v_{2,n}^R \end{bmatrix} \cos(n\omega t) + \begin{bmatrix} v_{1,n}^I \\ v_{2,n}^I \end{bmatrix} \sin(n\omega t) \right\} \tag{4-1}$$

and

$$\begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix} = \sum_{n=0}^{N} \left\{ \begin{bmatrix} i_{1,n}^R \\ i_{2,n}^R \end{bmatrix} \cos(n\omega t) + \begin{bmatrix} i_{1,n}^I \\ i_{2,n}^I \end{bmatrix} \sin(n\omega t) \right\} \tag{4-2}$$

where N is the maximum number of harmonics to be considered, and the superscripts R and I refer to the in-phase and quadrature components of the appropriate voltage and current harmonic amplitudes, respectively.

Additionally, since the first order time derivatives of the voltages are also required as input to the nonlinear MESFET model, equation (4-1) can be differentiated to obtain:

$$\frac{d}{dt} \begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \omega \sum_{n=1}^{N} n \left\{ \begin{bmatrix} v_{1,n}^I \\ v_{2,n}^I \end{bmatrix} \cos(n\omega t) - \begin{bmatrix} v_{1,n}^R \\ v_{2,n}^R \end{bmatrix} \sin(n\omega t) \right\} \tag{4-3}$$

The Fourier components:

$$\{v_{1,n}^{R},\ v_{1,n}^{I},\ v_{2,n}^{R},\ v_{2,n}^{I}\}_{n=0,1,\ldots N}$$

contain all of the terminal voltage information required by the nonlinear MESFET model.

The linear parasitic element network used in this work is shown in Figure 4.2. The elements are described in Section 2.2. The entire linear subnetwork (Figure 4.1) can be described in the frequency domain by a hybrid matrix of the form:

$$[H(n\omega)] \begin{bmatrix} V_1 \\ V_2 \\ i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} v_1 \\ v_2 \\ I_1 \\ I_2 \end{bmatrix} \qquad (4\text{-}4)$$

V_1 and V_2 are optional external voltage sources. All voltages and currents in the circuit are known once the steady-state interface currents, i_1 and i_2 are determined.

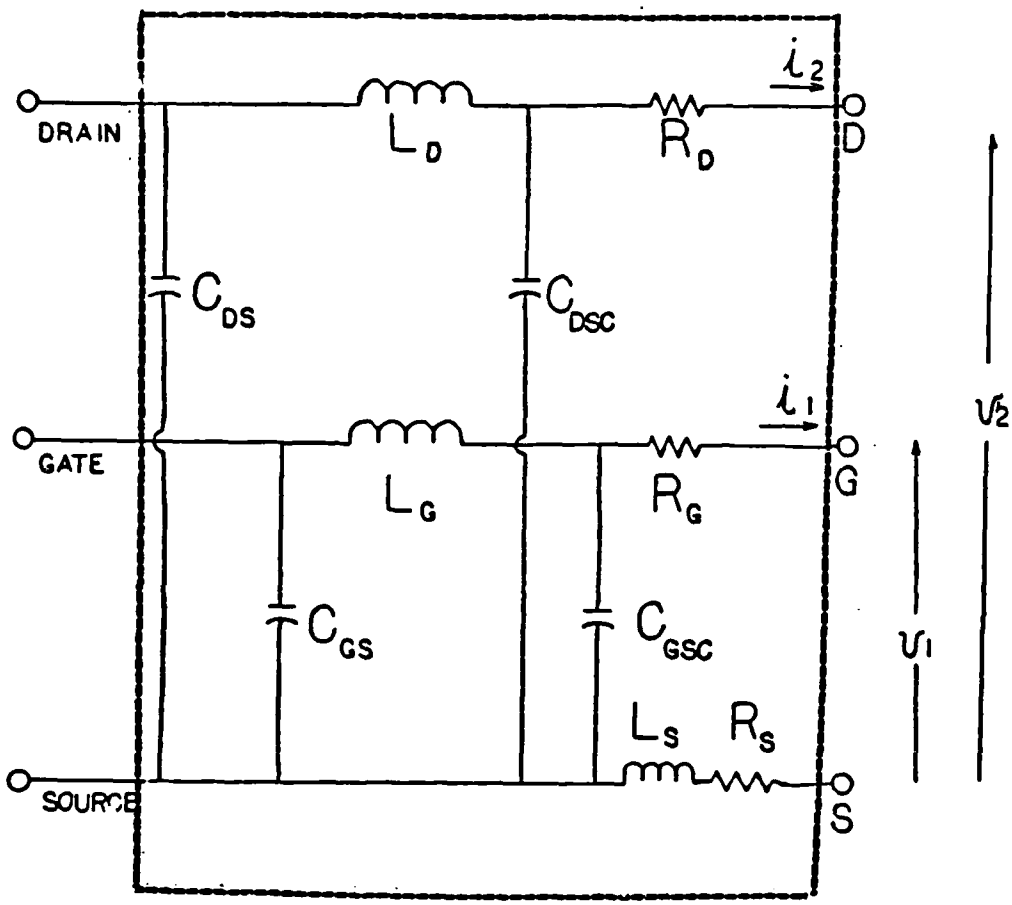

Figure 4.2. Linear parasitic element network. The nonlinear MESFET model is connected to the nodes at the right.

These currents, i_1 and i_2, are calculated using a nonlinear optimization algorithm. The procedure is as follows:

1.) The independent variables are the Fourier coefficients of the interface currents:

$$\{i_{1,n}^{R},\ i_{1,n}^{I},\ i_{2,n}^{R},\ i_{2,n}^{I}\}_{n=0,1,\ldots N}$$

An initial guess is assigned to these variables.

2.) The hybrid matrix describing the linear circuit is used to calculate the Fourier components of the interface voltages, v_1 and v_2.

3.) The Fourier components of the calculated interface voltages are used as input to the frequency-domain nonlinear MESFET which is described in the next section. This results in a second set of Fourier components for the interface currents:

$$\{i_{1,n}^{R*},\ i_{1,n}^{I*},\ i_{2,n}^{R*},\ i_{2,n}^{I*}\}_{n=0,1,\ldots n}$$

4.) An error function is defined:

$$E(\{i_{1,n}^{R},\ i_{1,n}^{I},\ i_{2,n}^{R},\ i_{2,n}^{I}\}_{n=0,1,\ldots N})$$

$$= \sum_{n=0}^{N} [(i_{1,n}^{R}-i_{1,n}^{R*})^2 + (i_{1,n}^{I}-i_{1,n}^{I*})^2 \qquad (4\text{-}5)$$

$$+ (i_{2,n}^{R}-i_{2,n}^{R*})^2 + (i_{2,n}^{I}-i_{2,n}^{I*})^2]$$

5.) The error function is iteratively minimized by a quasi-Newton optimizaton algorithm (67).

The entries in the hybrid matrix are calculated only once and stored for each frequency component. Consequently there is little computational expense associated with calculating the frequency-domain response of the linear part of the circuit to the interface currents. The key to the overall economy of the simulation algorithm is the efficient calculation of the interface currents resulting from the nonlinear MESFET model (step 3, above). Nakhla and Vlach (35) use numerical integration, such as described in Chapter 3, to the calculate the response of nonlinear subnetworks. This represents a considerable burden, since it must be done for each error function evaluation required by the optimization algorithm. The next section describes a scheme which eliminates the need for numerical integration.

4.2 EFFICIENT FREQUENCY-DOMAIN CHARACTERICATION OF THE NONLINEAR MESFET MODEL.

The circuit for the nonlinear MESFET model which was used for the time-domain simulations of Chapter 3 is shown in Figure 4.3. The drain, gate and source terminals are designated D, G and S, respectively. The equations for

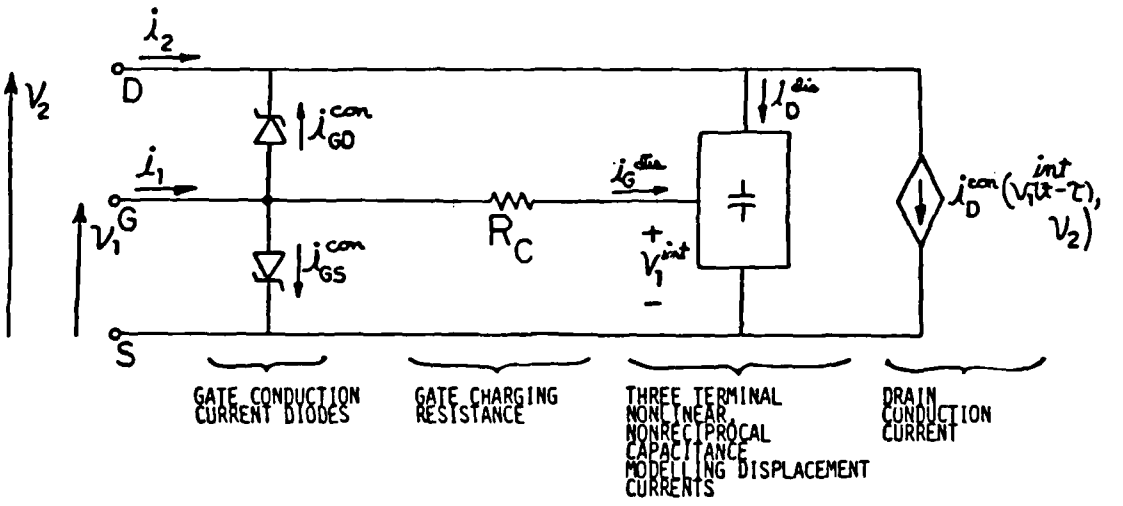

Figure 4.3. Nonlinear MESFET model with a gate charging resistance.

the drain and gate displacement currents are given in Figure 1.4. The diodes are added to model gate conduction current. It is desirable to calculate i_1 and i_2 explicitly from the terminal voltages v_1 and v_2, and their first order time derivatives. This is not possible because the presence of R_C, the gate charging resistance. The observation that the product of R_C and C_{11} is approximately constant and equal to 0.5τ, the electron transit time calculated by the MESFET model, motivated the replacement of R_C by a voltage delay of tau seconds as shown in Figure 4.4. The approximation, when compared with values obtained for R_C, is found to be good for values of v_2 greater than 0.1 V. This approximation was originally used by Madjar and Rosenbaum (28) to calculate R_C, and is expected to be good when electron velocity saturation effects dominate the FET's behavior, as indicated by drain current saturation. Scattering parameters (Section 2.2) calculated with both the R_C and time-delayed gate voltage versions of the model were not significantly different. (The impedance of a reactive element measured through a time-delayed voltage is demonstrated in Appendix 8.2.)

The use of a time-delayed gate voltage makes the explicit calculation of i_1 and i_2 possible because the Fourier components of v_1 are known. The expressions for the time delayed v_1 and its first order derivative with

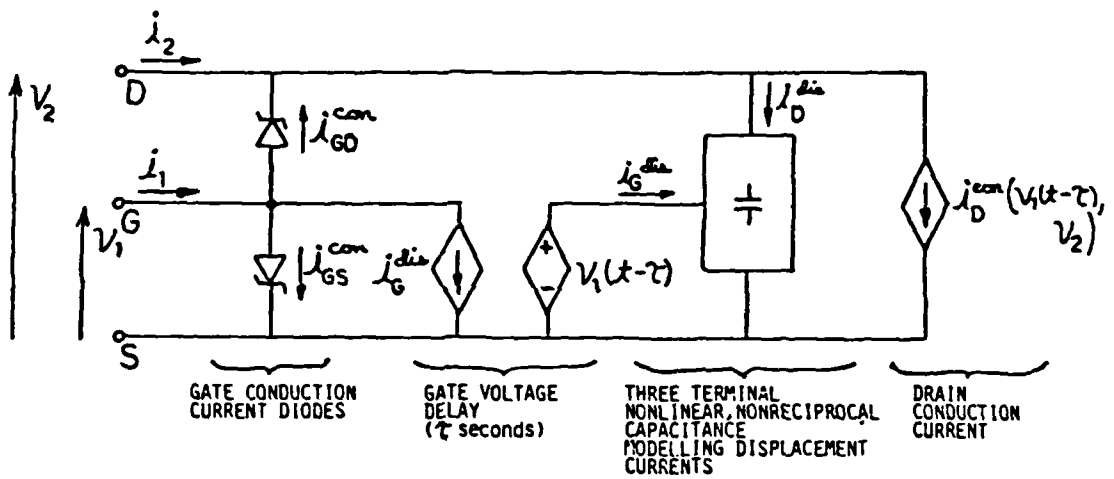

Figure 4.4. Explicitly nonlinear MESFET model with a time delay in the gate voltage.

respect to time are:

$$v_1(t-\tau) = \sum_{n=0}^{N} \left\{ v_{1,n}^{R} \cos[n\omega(t-\tau)] + v_{1,n}^{I} \sin[n\omega(t-\tau)] \right\} \quad (4.6)$$

and

$$\frac{dv_1(t-\tau)}{dt} = \omega \sum_{n=1}^{N} n\left\{ v_{1,n}^{I} \cos[n\omega(t-\tau)] - v_{1,n}^{R} \sin[n\omega(t-\tau)] \right\} \quad (4.7)$$

The sequence for evaluating the frequency-domain interface current response of the nonlinear MESFET model to the frequency-domain interface voltages (Step 3 in Section 4.1) is illustrated in Figure 4.5. The Fourier components of the interface voltages are translated into time-domain samples over one period using equations 4.1, 4.2, 4.3, 4.6, and 4.7. The minimum number of time samples per fundamental period is determined by the Nyquist sampling theorem (68) to be twice the number of the highest harmonic. These interface voltages, time delayed voltages, and first order derivatives with respect to time are used as input to the nonlinear MESFET model which returns gate and drain current values for the same time samples. These interface current samples are then

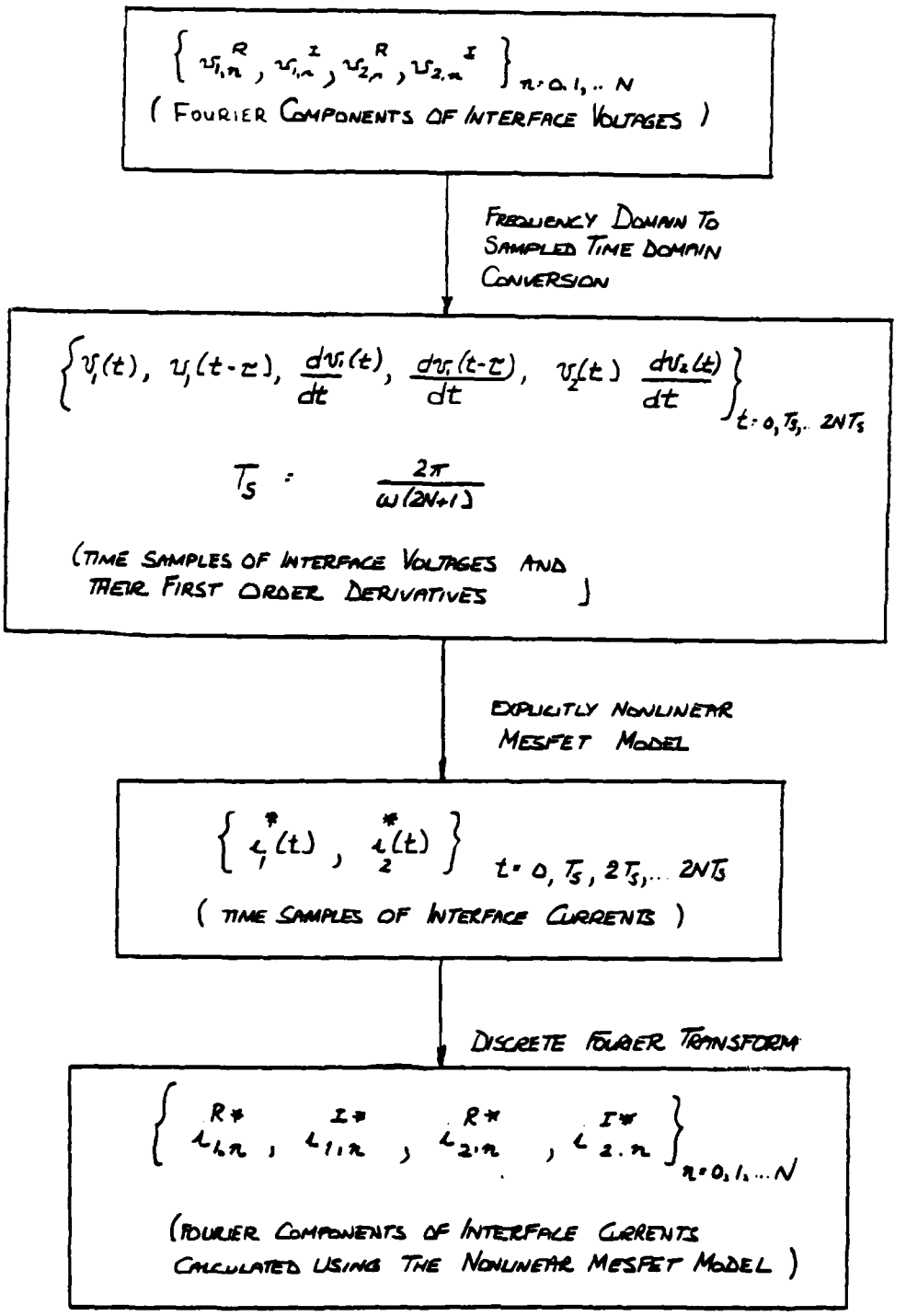

Figure 4.5. Frequency-domain characterization of the explicitly nonlinear MESFET model.

converted back to Fourier components using a discrete Fourier transform (62). The number of sample points per period is set at fifteen, which allows a maximum of seven harmonics to be considered. The sine and cosine coefficients for the frequency to time domain conversion, and the discrete Fourier transform are calculated only once and stored, after the fundamental frequency has been selected, and the transit time, τ, has been obtained from the MESFET model.

4.3 FREQUENCY-DOMAIN SIMULATION ALGORITHM PERFORMANCE

The frequency-domain simulation program was tested at each stage of its development. Initially the nonlinear MESFET model was replaced with a linear resistive network with no frequency- to time-domain interconversion in order to debug the linear network and nonlinear optimization parts of the software. Next, the frequency to time domain interconversion software was included. Performance was investigated with simple analytic nonlinearities. And finally, the nonlinear MESFET model completed the package which was used for the overdriven amplifier simulations of Section 5.2.

Initially, the optimization algorithm proceeded in stages. The D.C. problem was solved first, and the harmonics were included one by one, making use of the

interface current solutions from the previous step as initial guesses. However, it was found to be more economical to include all of the harmonics to be considered in one optimization attempt. Overdriven MESFET amplifier simulations including harmonics through the second typically require fewer than one thousand error function evaluations - depending on bias voltages and drive level. Simulations including harmonics through the sixth were performed with fewer than three thousand error function evaluations, however the magnitudes of the interface currents at and above the fourth harmonic were more than five orders of magnitude below the fundamental current magnitudes. The number of independent variables in the optimization is four times the number of the highest harmonic being considered. If the highest harmonic being considered is the second, the frequency-domain simulation algorithm is more efficient than the numerical integration technique used in Chapter 3 for solving for steady-state solutions. The advantage would be even greater for circuits containing more complicated linear subnetworks, and no problems are presented by the presence of vastly differing time constants such as those associated with the use of realistic biasing networks.

5. THE OVERDRIVEN MESFET AMPLIFIER

The NE869177 MESFET which is described in Chapters 1 and 2 was used in a common-source amplifier circuit for experiments in which output power at the first and second harmonics was measured as a function of input drive at different gate bias voltages. The D.C. components of the gate and drain currents were simultaneously measured through the biasing network. The experimental results will be compared with simulated results obtained using the nonlinear MESFET model in conjunction with the large-signal frequency-domain circuit simulation method presented in Chapter 4. This was done to further test the validity of the nonlinear MESFET model for large-signal simulation and design purposes. Additionally, simulations were performed both with and without reverse breakdown gate current in order to investigate the claim made by Sechi, Huang and Perlman (61) that such breakdown current plays an important role in gain saturation for power MESFETs.

5.1 OVERDRIVEN MESFET AMPLIFIER EXPERIMENTS

The 0.5 micron gate length NE869177 MESFET which is described in Table 2.2 and illustrated in Figure 1.2 was mounted for the amplifier experiments as pictured in

Figure 5.1. The 50 ohm microstrip lines at the gate-source and drain-source ports of the NEC type 77 carrier were connected to SMA coaxial connectors through additonal lengths of 50 ohm microstrip into which were incorporated biasing networks consisting of 120 pF D.C. blocking capacitors and high impedance branch lines. The gate and drain tuning stubs supplied by the manufacturer on the MESFET carrier were empirically adjusted for maximum small-signal gain at 10 GHz, with the gate-source bias at -3.00 volts and the drain-source bias at 7.50 volts.

The remainder of the test apparatus (Figure 5.2) was constructed with X-band (WR-90) waveguide components. These components were calibrated for power measurements at 20 GHz, the second harmonic. At 10 GHz incident, reflected and output power was measured using a General Microwave Corporation model N420B thermoelectric X-band power head. The error introduced by the presence of the second harmonic was less than one percent because of low second harmonic power levels which were further reduced by inefficient coupling through the X-band components. 20 GHz power measurements were made with a calibrated Tektronix 491 spectrum analyzer and Ku-band waveguide mixer in conjunction with a precision Hewlett-Packard Ku-band variable attenuator which was adjusted for constant spectrum analyzer display readings. A X-band to

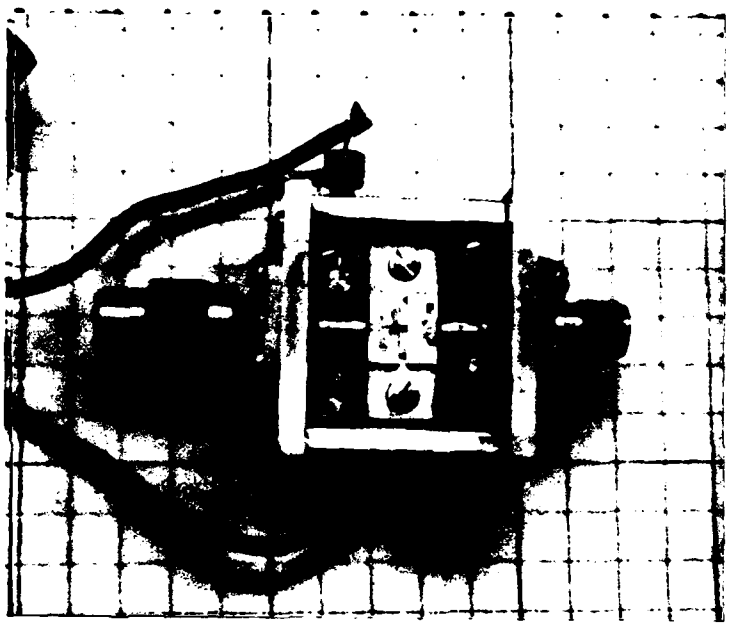

Figure 5.1. NE869177 MESFET mounted for use in amplifier experiments. The gate-source port is on the left. Grid squares are 0.2 inches across.

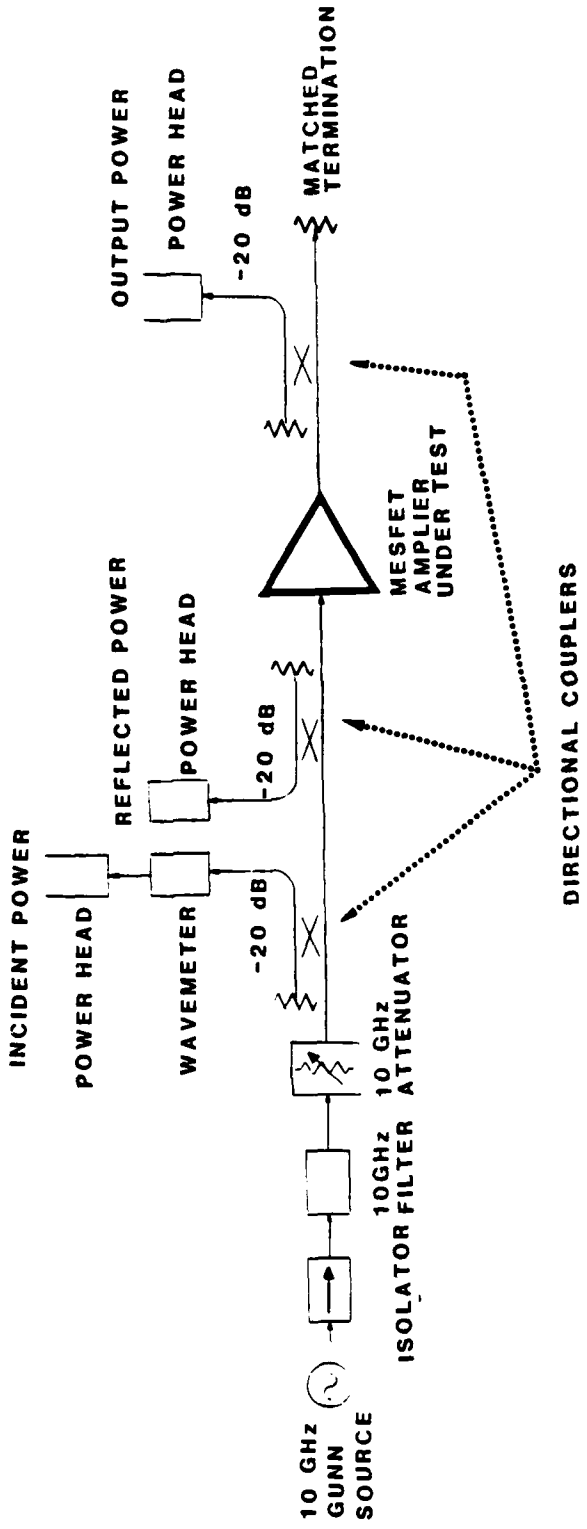

Figure 5.2. Apparatus used for the overdriven amplifier experiments (X-band waveguide used throughout.)

K_u-band waveguide taper was used to mount this combination in place of the X-band power heads, and effectively prevented first harmonic power from reaching the mixer since 10 GHz is below the K_u-band cutoff frequency. The Tektronix 491 spectrum analyzer was calibrated for 20 GHz power measurements using a General Microwave Corporation model K420C Ku-band thermoelectric power head.

The amplifier was mounted in the waveguide apparatus using X-band waveguide-to-coax adaptors which present 50 ohm impedances to the amplifier at 10 GHz. Although power transmission and reflection coefficient magnitudes for these adaptors were measured at 20 GHz, there was no equipment available to measure the angles.

Gate-source and drain-source bias voltages were supplied by separate power supplies. These voltages and the D.C. currents were monitored with Hewlett-Packard 3466A digital multimeters. The open MESFET chip was shielded from room light because this was observed to affect drain current readings , especially at larger negative gate-source bias voltages.

Figures 5.3 through 5.7 present measurements taken as functions of the 10 GHz input power delivered to the gate-source port of the MESFET amplifier. The drain-source bias voltage was 7.50 volts in all cases. The gate-source bias voltage was varied between -1.00 and -5.00 volts in one volt increments. The input power was

calculated by subtracting the 10 GHz reflected power from the incident power. Figure 5.3 displays the 10 GHz output power, measured at the drain source port. Figure 5.4 shows the second harmonic output power, and Figure 5.5 presents the second harmonic power measured out of the amplifier's input (gate-source port). Figures 5.6 and 5.7 present D.C. drain and gate currents, respectively.

For -5.00 volts gate-source bias, the D.C. (i.e. average) component of the drain current (Figure 5.6) increases with input power. This is expected for Class B operation, with the MESFET cut-off for about half a cycle because of the nonlinear drain current characteristic (Figure 2.7). A similar argument explains the D.C. drain current rise at -4.00 volts gate-source bias. For gate-source biases of -1.00 and -2.00 volts, the D.C. drain current decreases with increasing drive level. This is also expected as forward gate conduction results in drain current waveform clipping. The observation that the D.C. drain current remains relatively constant at a gate-source bias of -3 volts indicates that the drain current waveforms are more symmetrically limited by a combination of gate conduction and drain current cut-off.

The D.C. gate current measurements (Figure 5.7) show negative current which increases in magnitude with the 10 GHz input power for gate-source bias voltages of -3.00 through -5.00 volts. This would be expected from

avalanche breakdown reverse gate current occuring during negative maxima in the gate-source voltage waveforms. There is an abrupt increase in positive D.C. gate current with input drive at -1.00 volt gate-source bias, resulting from the Schottky barrier gate being driven into forward conduction for part of each cycle. The curve for -2.00 volts indicates a combination of reverse breakdown and forward conduction current through the gate, with forward conduction dominating at the higher power levels.

The 10 GHz output power curves (Figure 5.3) at -1.00 volt gate-source bias saturates earliest, probably because of forward gate conduction. This will be investigated in the simulation in the next sections. The -5.00 volt gate-source bias curve is concave upward - the gain increases with input drive. This would not be expected if reverse gate breakdown current were a dominating factor in gain saturation.

The second harmonic power curves (Figures 5.4 and 5.5) are more complicated than the fundamental power curves. Such behavior is typical of the second harmonic component of sine-wave tips transformed through a square-law nonlinearity as the conduction angle increases (69). The second harmonic power at the drain-source port of the transistor is greatest for gate-source biases of -1.00 and -2.00 volts, where forward gate conduction would be expected to play a significant role in harmonic

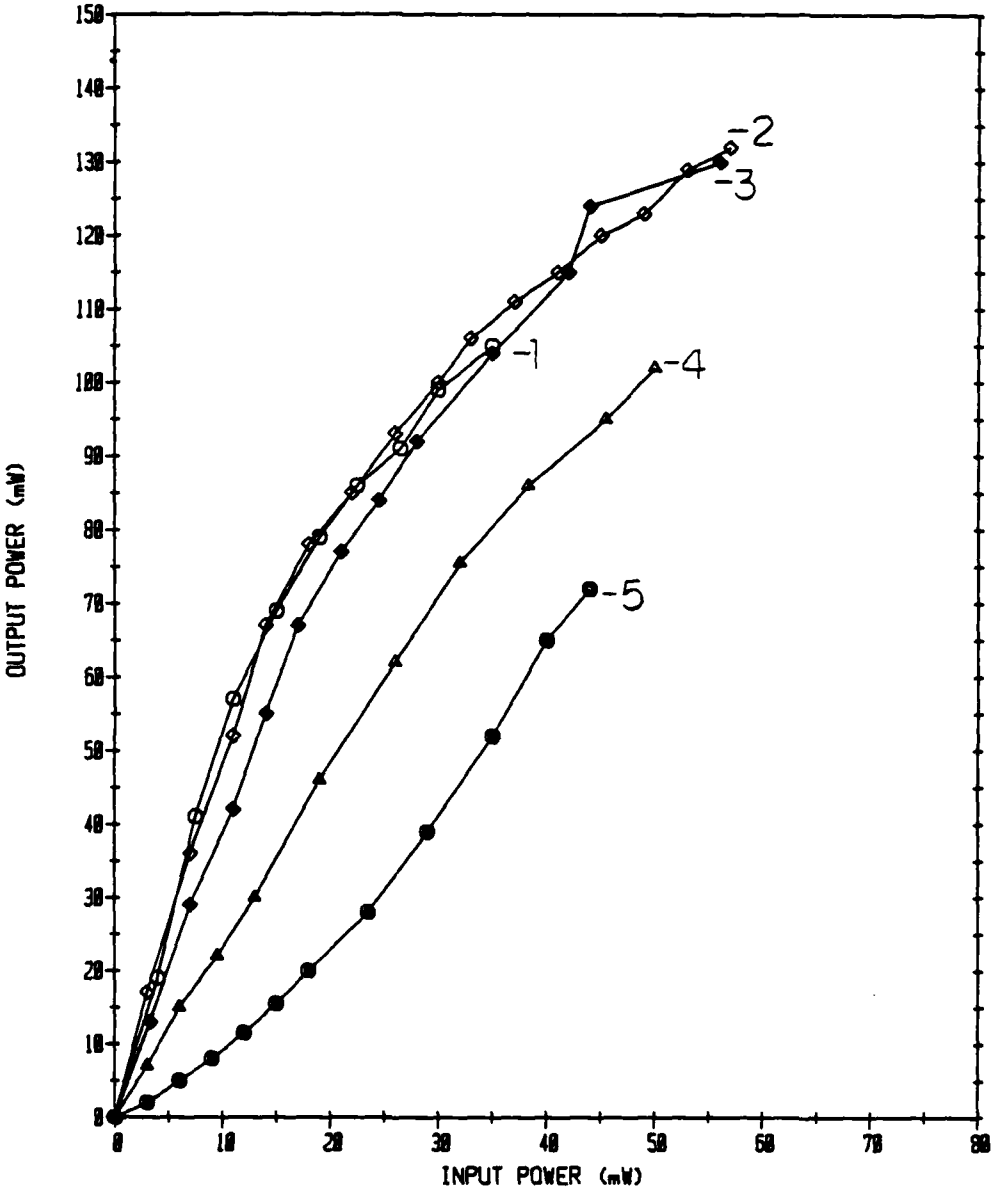

Figure 5.3. MESFET amplifier 10 GHz output power as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves.

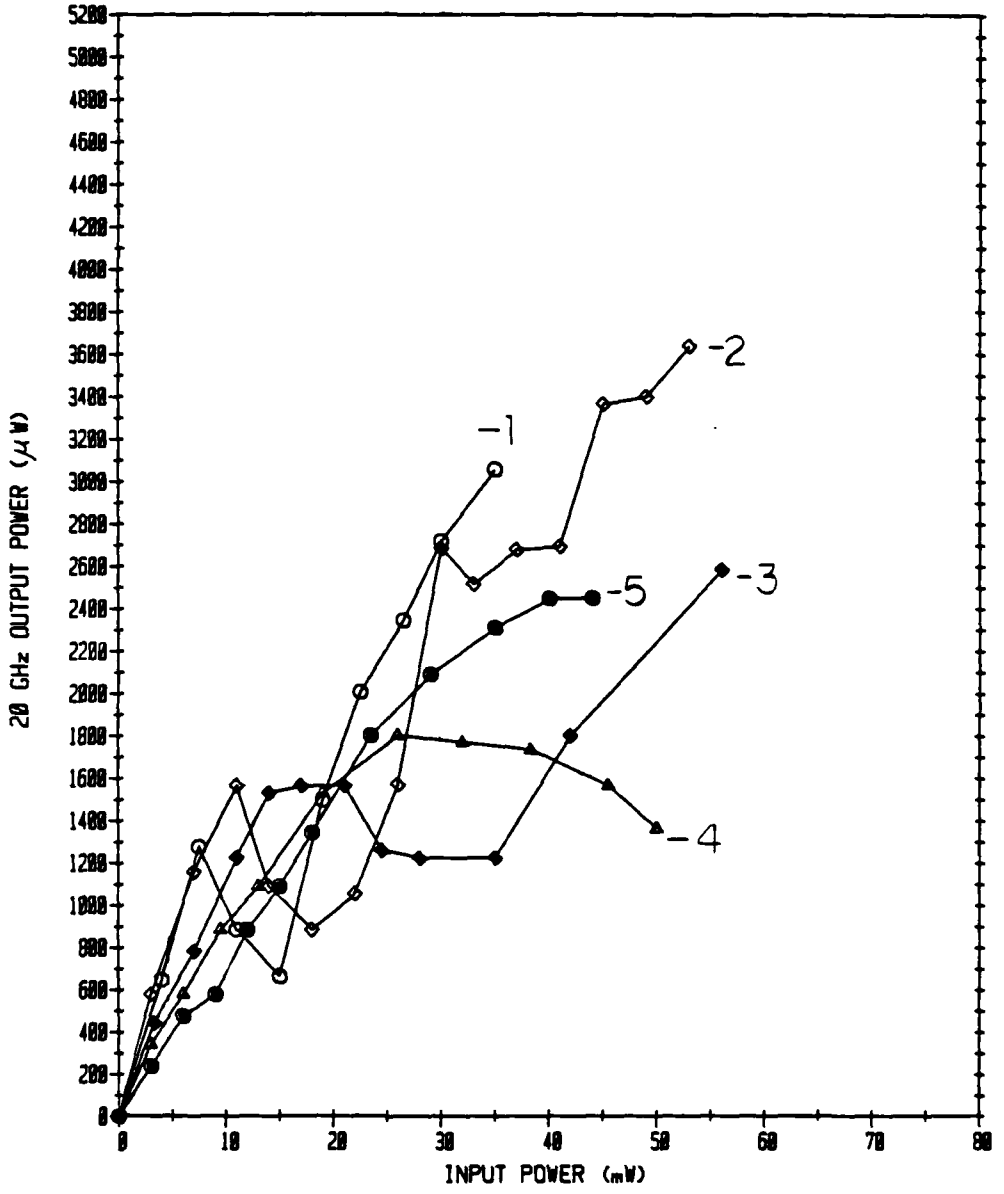

Figure 5.4. MESFET amplifier 20 GHz output power as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves.

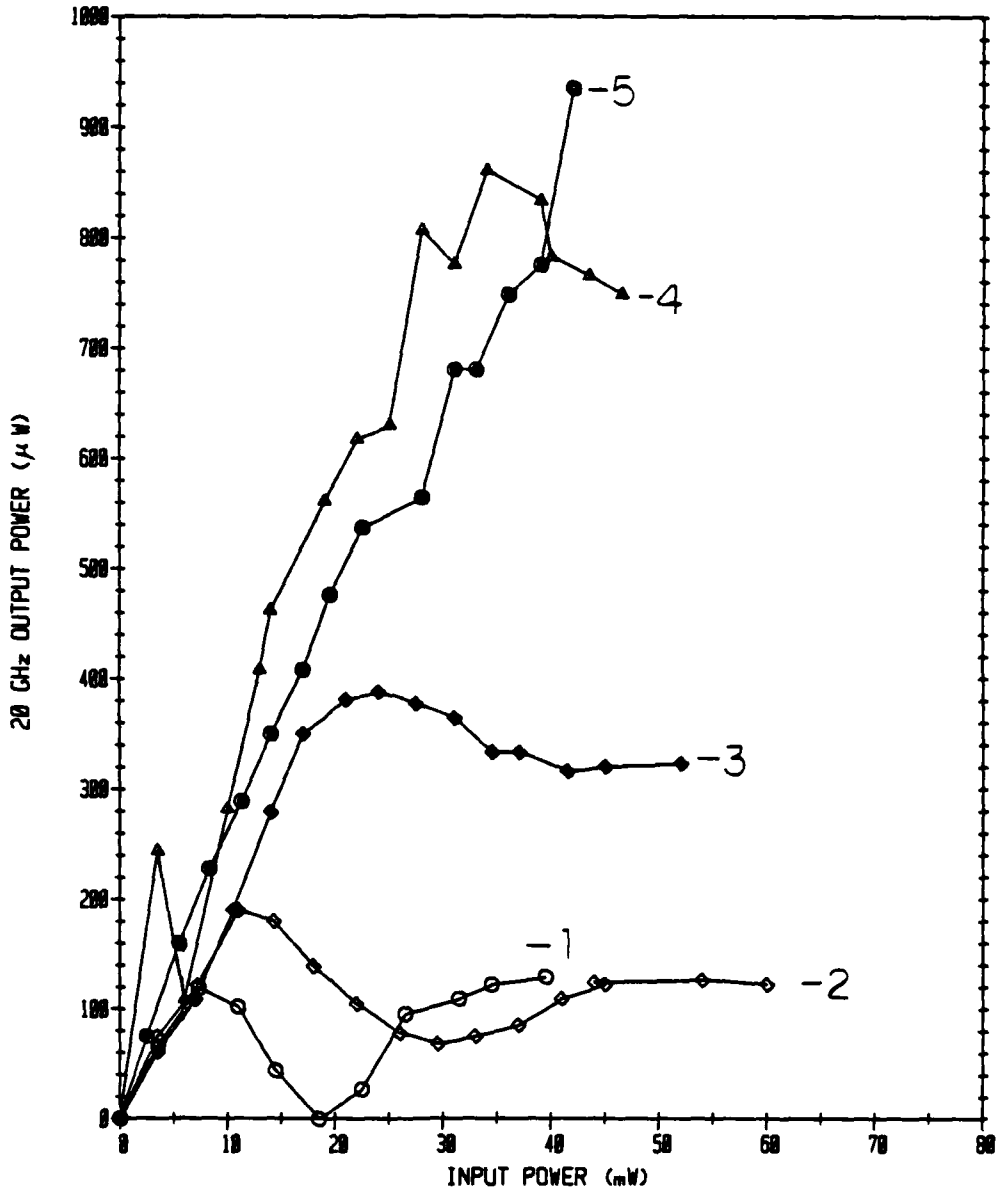

Figure 5.5. MESFET amplifier 20 GHz power out of the gate-source port as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves.

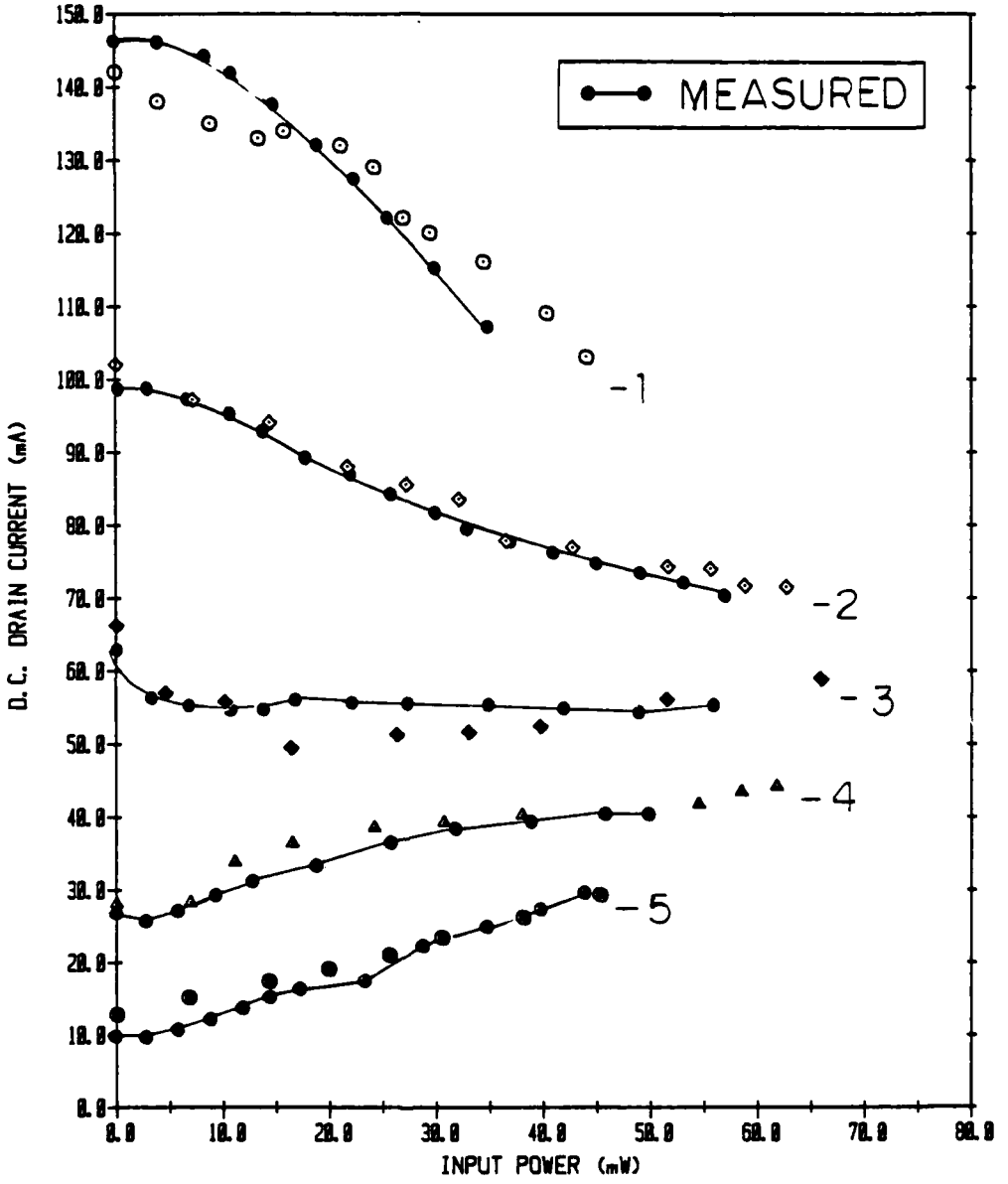

Figure 5.6. MESFET amplifier D.C. component of drain current as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves. (Measured and simulated.)

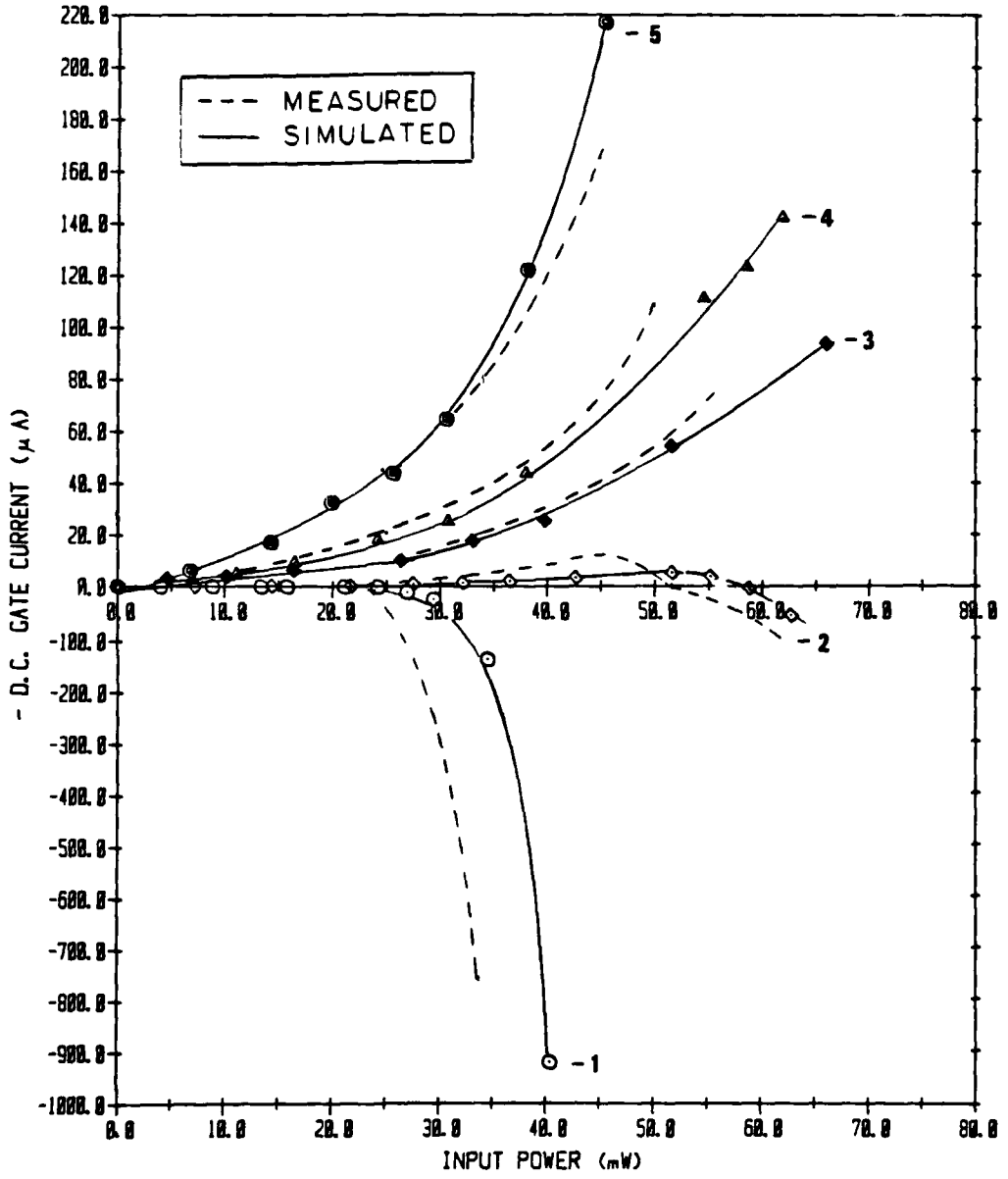

Figure 5.7. MESFET amplifier D.C. component of gate current as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves. (Measured and simulated.)

generation. The opposite is true for the second harmonic power measured at the gate-source port (Figure 5.5). Here, the highest powers are observed at gate-source biases of -5.00 and -4.00 volts where drain current cutoff during part of each cycle is more important. In general, the 20 GHz power measured at the drain-source port is about five times as great as that measured at the gate-source port, and is two orders of magnitude below the fundamental output power.

5.2 OVERDRIVEN AMPLIFIER SIMULATION

The circuit for the overdriven MESFET amplifier simulations is illustrated in Figure 5.8. Not shown is the ideal biasing network which supplies D.C. bias voltages directly to the gate-source and gate-drain terminals. The packaged MESFET consists of the nonlinear MESFET model of Figure 4.4 and the linear parasitic element network of Figure 4.2. The material and geometric parameters for the nonlinear model are given in Table 2.2, and the linear parasitic element values are presented in Table 2.3.

Figure 5.9 is the piecewise-linear I-V characteristic used for the gate conduction current diodes (Figure 4.4). The open circles represent experimental reverse gate current measurements for the NE869177 MESFET.

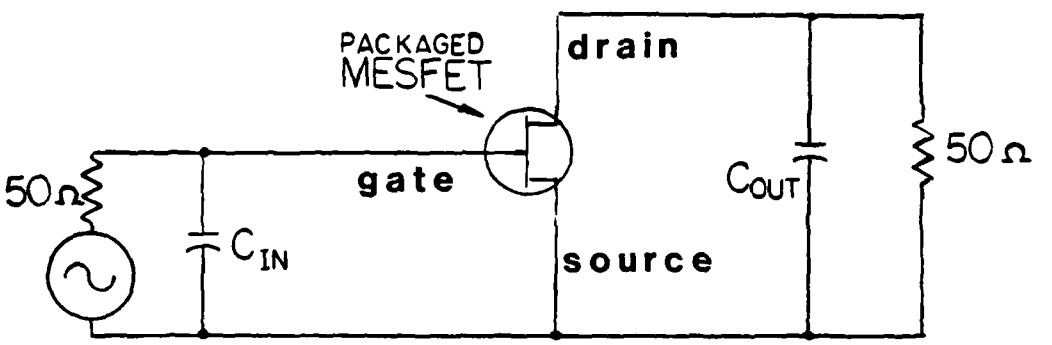

Figure 5.8. Circuit for overdriven MESFET amplifier simulations.

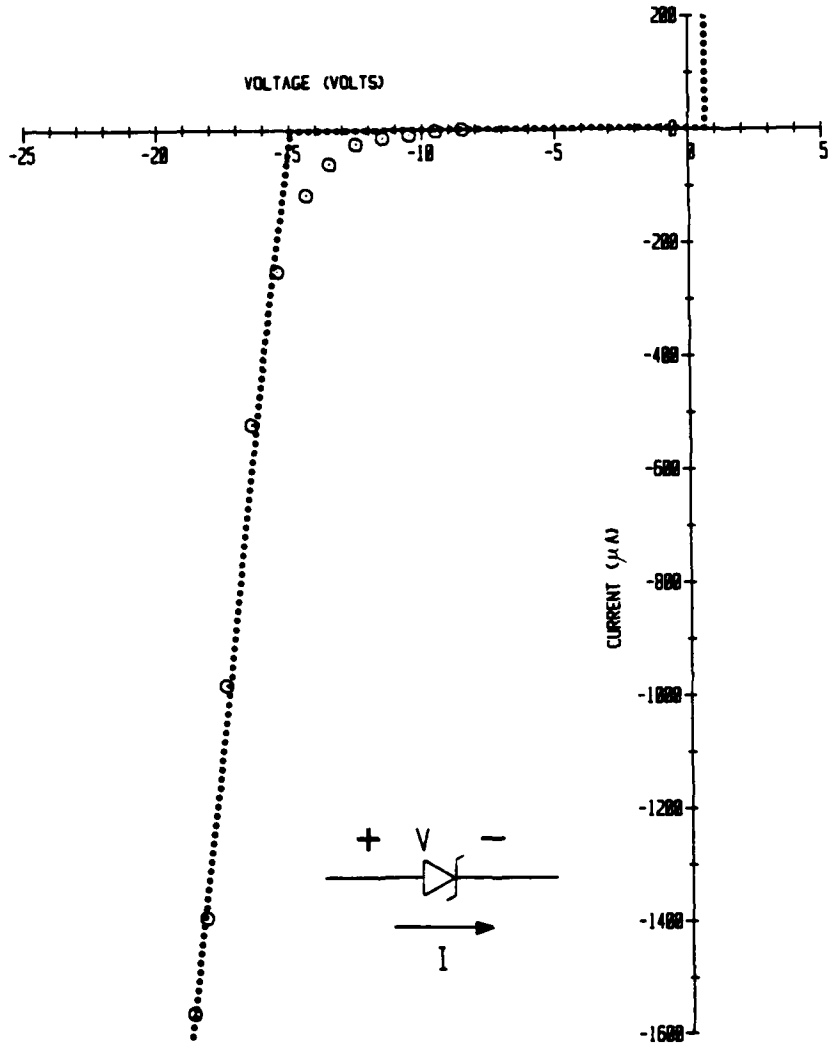

Figure 5.9. Gate conduction current diode model static I-V characteristics. (Measured and piecewise-linear approximation.)

The gate current was measured as a function of gate-source voltage, as the drain-source voltage was held at -7.5 V. For negative gate-source bias, the gate-drain diode has a larger negative voltage across it than the gate-source diode due to the drain-source bias, consequently, most of the measured reverse current is due to conduction through the gate-drain diode. The same I-V characteristic is used for both the gate-drain and gate-source diodes in Figure 4.4. For the piecewise-linear approximation, the forward turn-on voltage is 0.7 V, at which point the diode resistance drops to zero. The reverse turn-on voltage is -15 V, at which point the diode conductance becomes 0.49 millimhos.

The large-signal frequency-domain circuit simulation technique described in Chapter 4 was used to obtain steady-state responses. The capacitors, C_{IN} and C_{OUT} (Figure 5.8), model reactances associated with the tuning stubs and microstrip to SMA adaptors in the actual amplifier (Figure 5.1). The values for these capacitances are difficult to calculate or precisely measure; consequently, they were determined by conducting simulations and adjusting them for maximum small signal gain for a gate-source D.C. bias voltage of -3.00 V, and a drain-source bias of 7.50 V, as was done when the actual amplifier was experimentally tuned. The values determined for C_{IN} and C_{OUT} are 0.4 pF and 0.3 pF, respectively.

Using these capacitance values, simulations were performed over a range of input power levels in order to compare with the experiments presented in the preceding section. The temperature specified to the nonlinear MESFET model for lookup table generation was manually adjusted to match the calculated power dissipation in the simulation to within 10 percent. Figure 5.10 presents the simulated 10 GHz output power results.

It was found necessary to adjust the reactances represented by C_{IN} and C_{OUT} at the second harmonic in order to achieve agreement with the general shapes of the measured curves for the second harmonic output power (Figure 5.11). Because the linear subnetwork response in the frequency-domain simulation algorithm is calculated independently at each frequency component, frequency sensitive capacitances present no problem. It is not surprising that the reactances due to the tuning stubs and transitions in the actual amplifier are not adequately represented by single simple elements. The values obtained for C_{IN} and C_{OUT} at 20 GHz are 0.8 pF and 0.5 pF, respectively, and the values at 10 GHz were not changed. The simulated 20 GHz output power results are shown in Figure 5.11, and the 20 GHz power out of the gate-source port is displayed in Figure 5.12.

Figure 5.13 compares measured and simulated 10 GHz output power results. Agreement for the -1 V gate-source

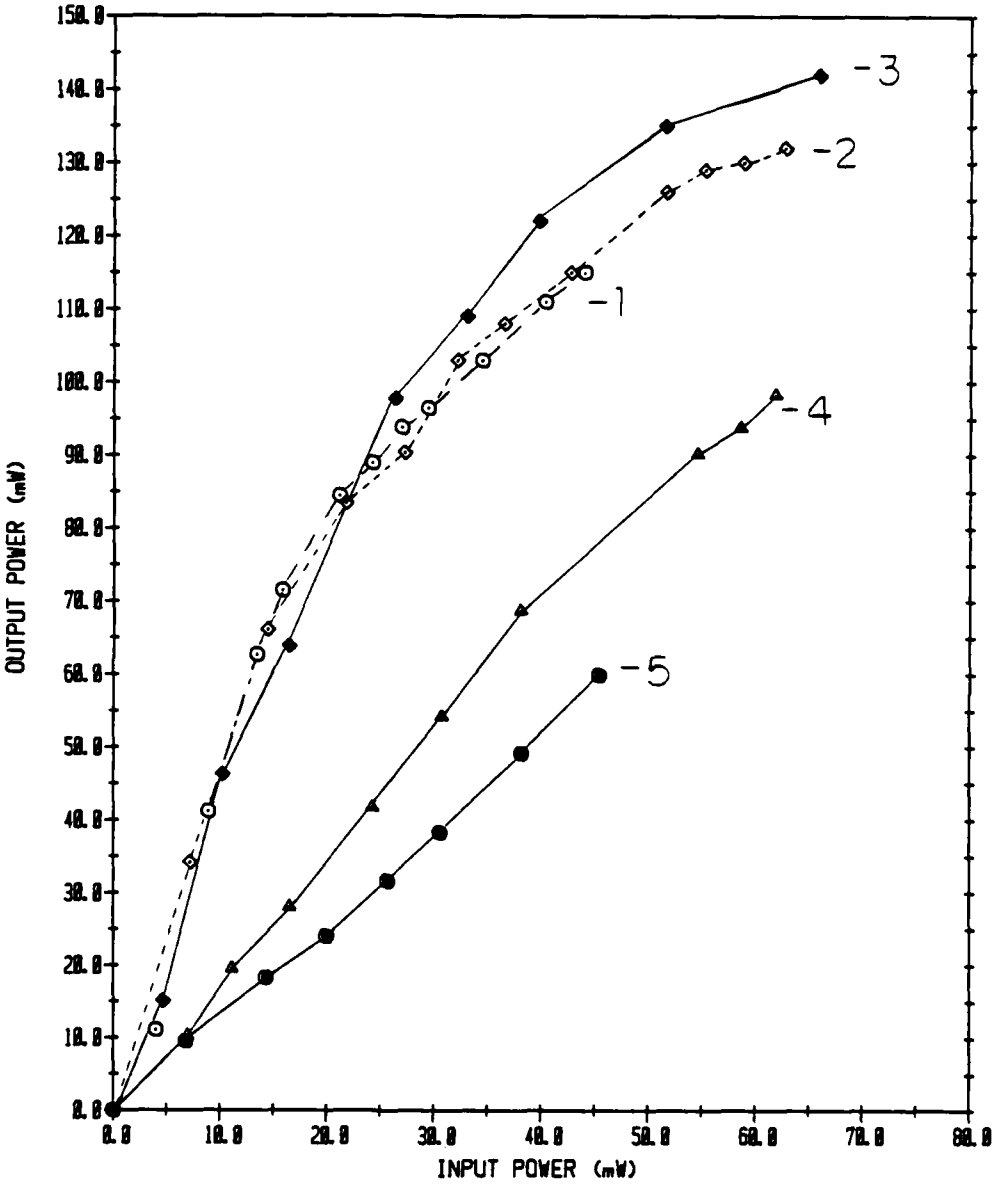

Figure 5.10. Simulated MESFET amplifier 10 GHz output power as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves.

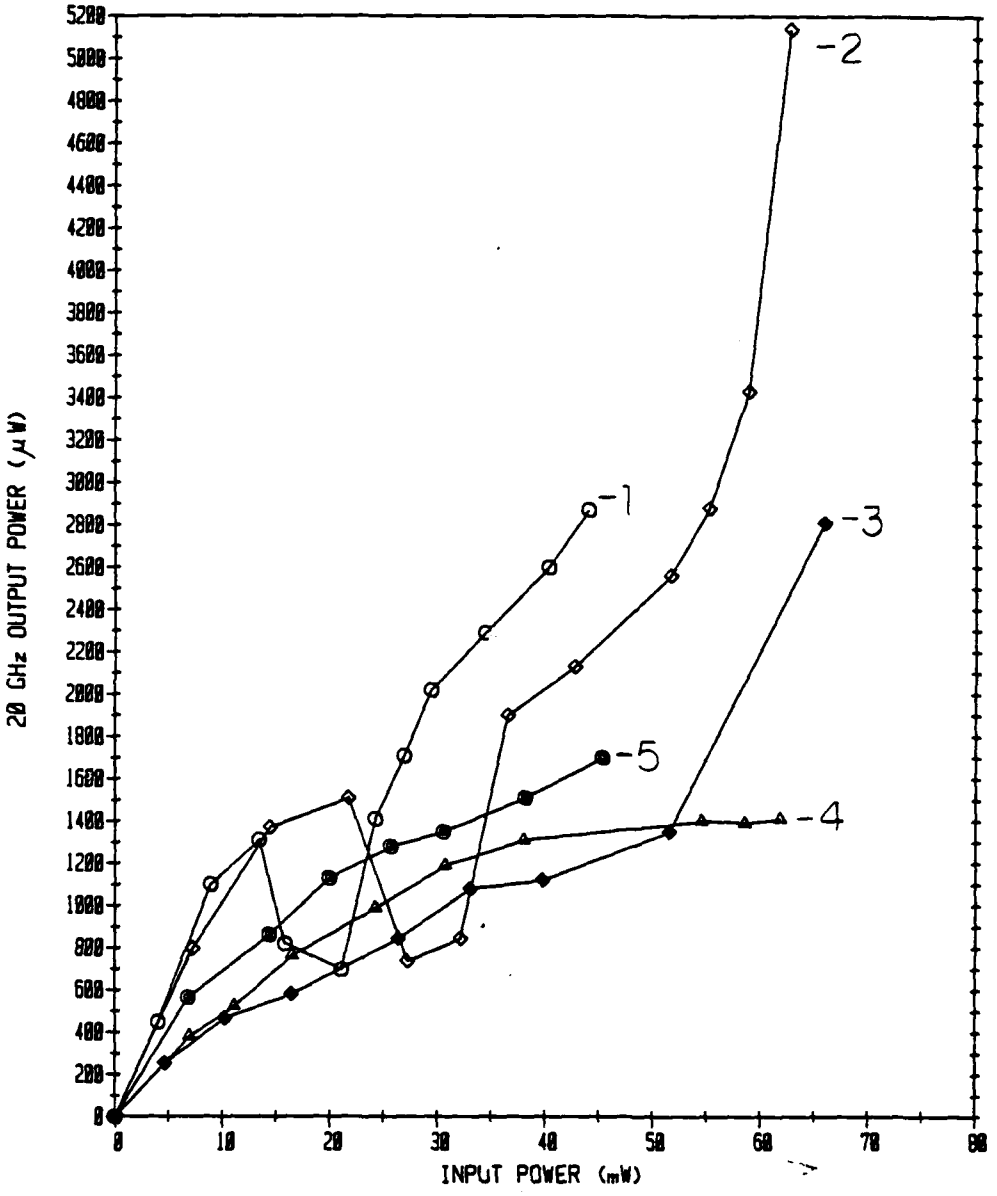

Figure 5.11. Simulated MESFET amplifier 20 GHz output power as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves.

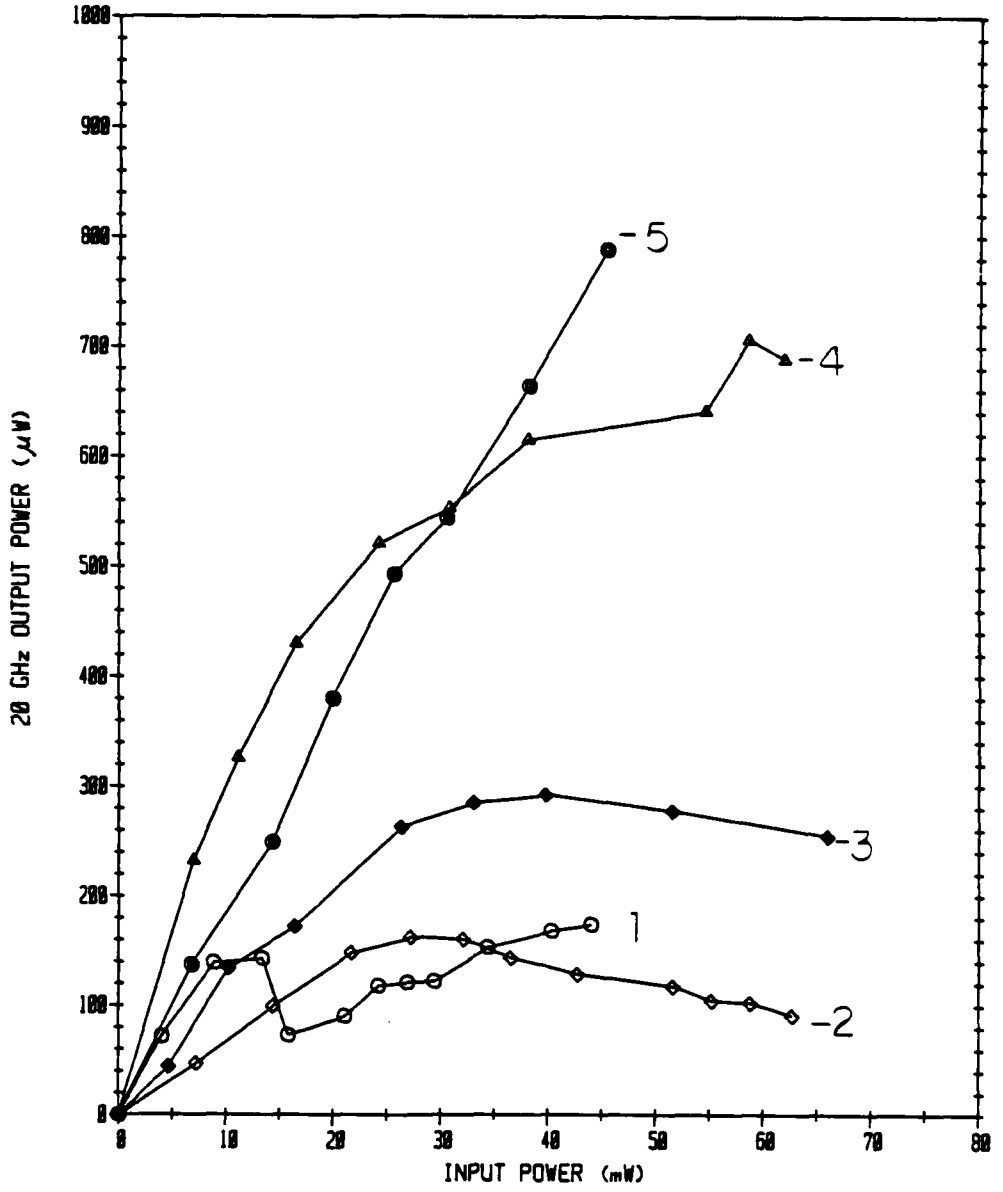

Figure 5.12. MESFET amplifier 20 GHz power out of the gate-source port as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves.

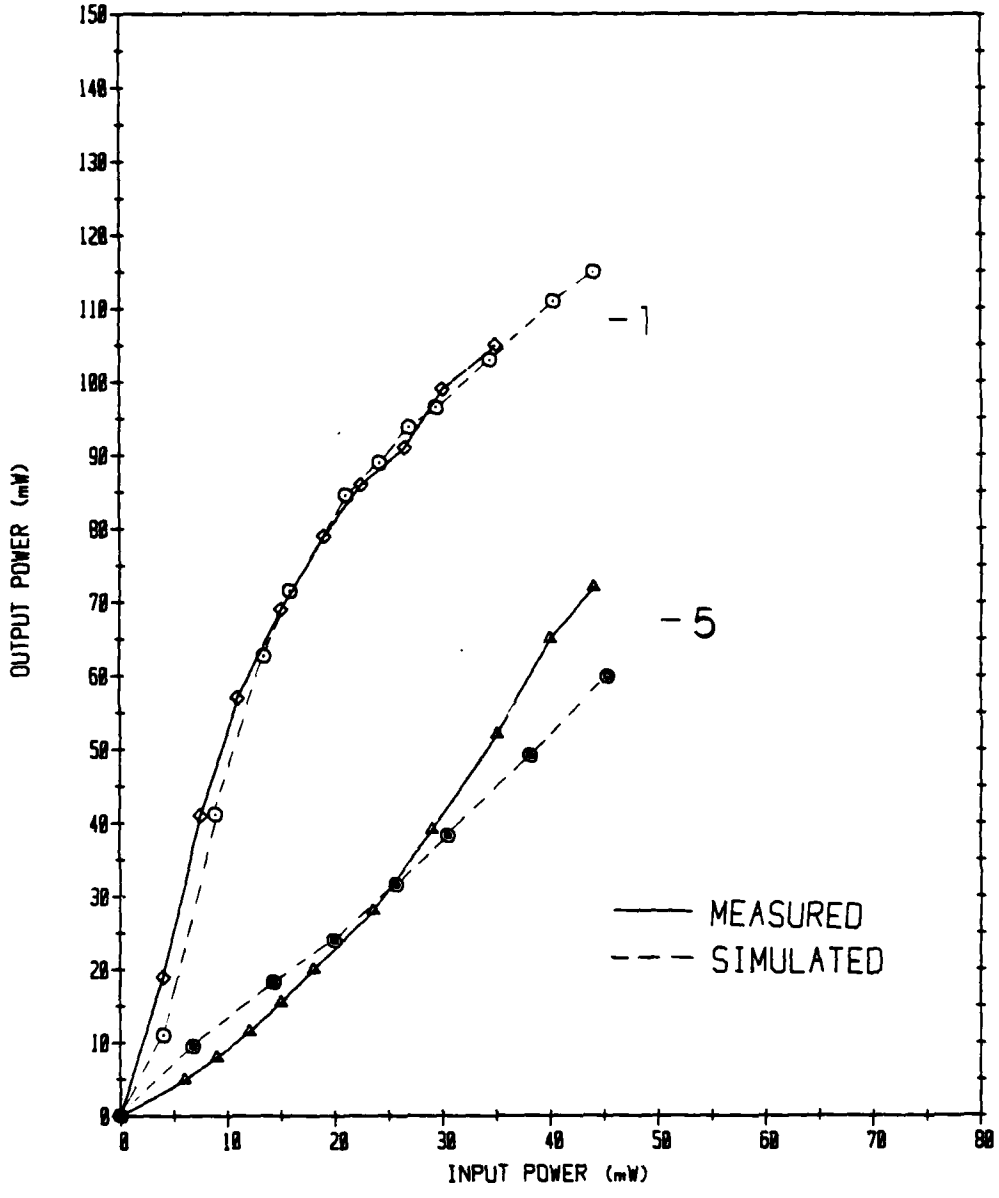

Figure 5.13. Comparison of measured and simulated MESFET amplifier 10 GHZ output power as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves.

bias is excellent, and the agreement for -5 V is better than 1 dB. Figure 5.14 compares simulated and measured 20 GHz power out of the drain-source port. Again, the agreement is reasonable, better than 1.6 dB, and the shapes of the curves are similar. Figures 5.6 and 5.7 compare measured and simulated D.C. drain and gate currents. Good correspondance is also observed here.

On the basis of these comparisons, the nonlinear MESFET model together with the large-signal, frequency domain, steady-state simulation algorithm appear adequate for large-signal design applications. If time-domain waveforms and limit cycles such as presented in Chapter 3 are desired, they can be constructed from voltage and current frequency components provided by the simulation algorithm. Figure 5.15 presents gate and drain current waveforms (at the MESFET chip) constructed from a simulation including the first three harmonics. These waveforms are not as detailed as those resulting from time-domain numerical integration (Figure 3.21 for example), however one must exercise caution in the interpretation of sharp details since they may represent frequency components beyond the valid range of the MESFET model.

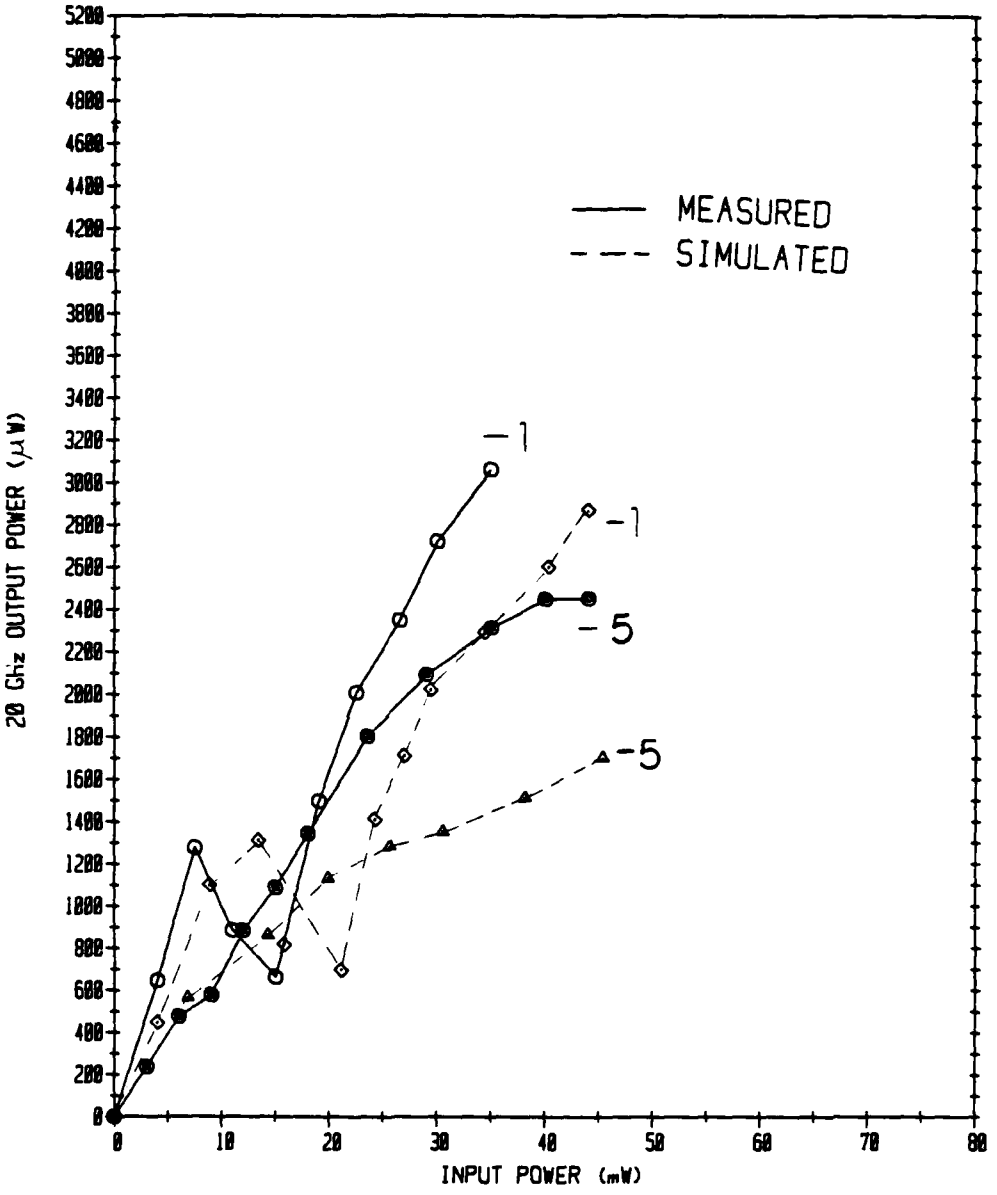

Figure 5.14 Comparison of measured and simulated MESFET amplifier 20 GHz output power as a function of 10 GHz input power. Drain-source bias voltage: 7.50 V. The gate-source bias voltages are indicated next to the curves.

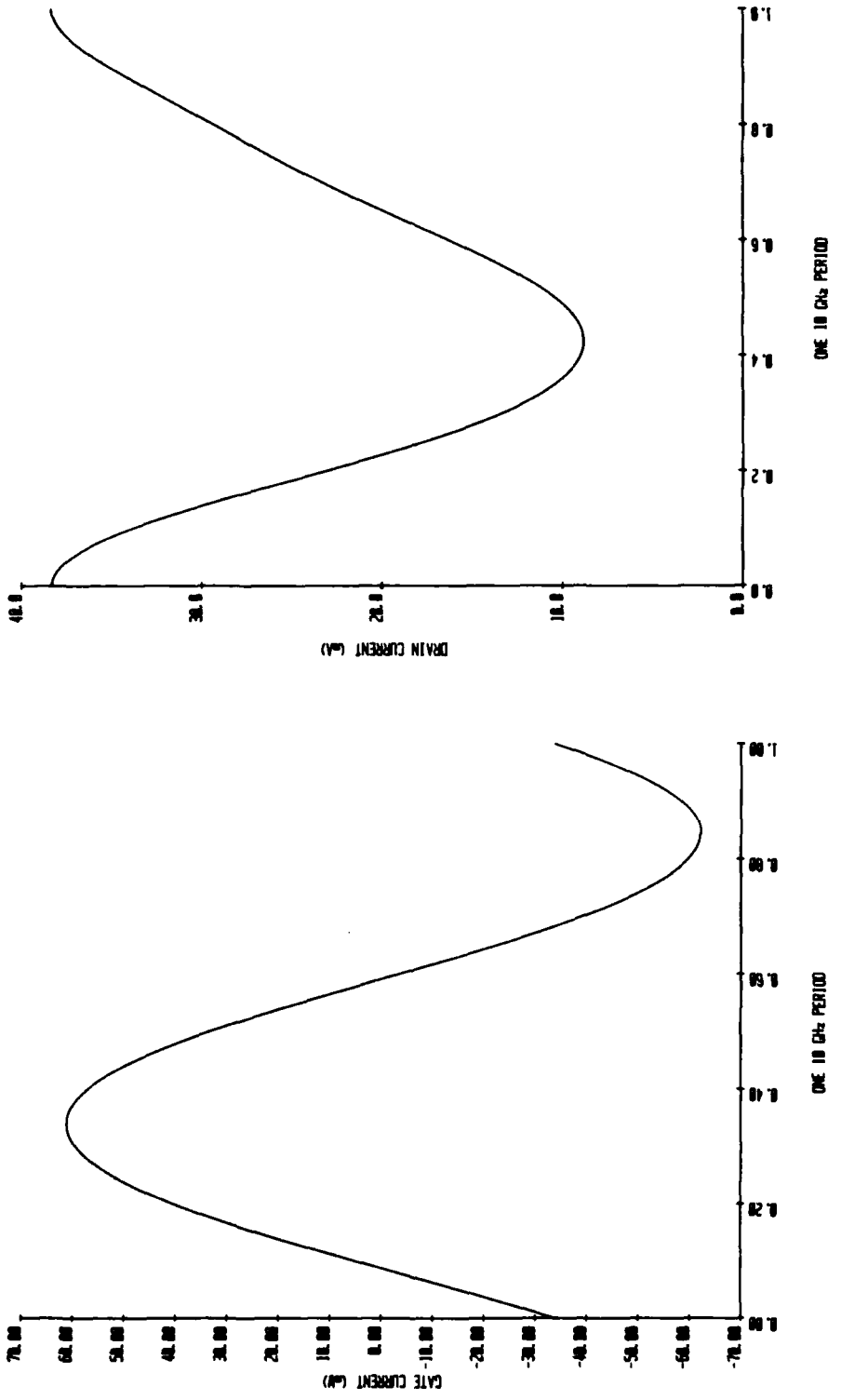

Figure 5.15. Simulated gate and drain current waveforms for the overdriven MESFET amplifier. Drain-source bias: 7.50 V. Gate-source bias: -5.00 V. 10 GHz input power: 34 mW.

5.3 GATE BREAKDOWN AND GAIN SATURATION

Sechi, Huang and Perlman (61) have conducted power and sampled waveform measurements on an overdriven MESFET amplifier operating at 3 GHz, and have come to the conclusion that nondestructive reverse gate breakdown current is responsible for gain saturation in power MESFETs. Although their experiments indicate that gate breakdown and current saturation may occur concurrently, they cannot establish a clear cause-effect relationship. This is important for device designers.

The amplifier experiments reported in Section 5.1 cast some initial doubt on the Sechi et. al. hypothesis. As the D.C. gate-source voltage is made more negative, the reverse D.C. current through the gate increases (Figure 5.7) indicating more gate breakdown. However, the 10 GHz output power curves (Figure 5.3) do not indicate the expected corresponding decrease in the onset of gain saturation with increasing negative gate-source bias.

A cause-effect relationship between gate breakdown and gain saturation can be investigated using the MESFET model by simply comparing large-signal simulations performed with and without gate breakdown. Gate breakdown was eliminated by setting the reverse breakdown voltage for the diode I-V characteristic (Figure 5.9) to -1000 V.

Simulated 10 GHz output power with and without gate breakdown current is presented in Figure 5.16. The gate-source bias voltage for the simulations is -5.00 V, where the breakdown current is greatest (Figure 5.7). The elimination of the gate breakdown current has no discernable effect on the output.

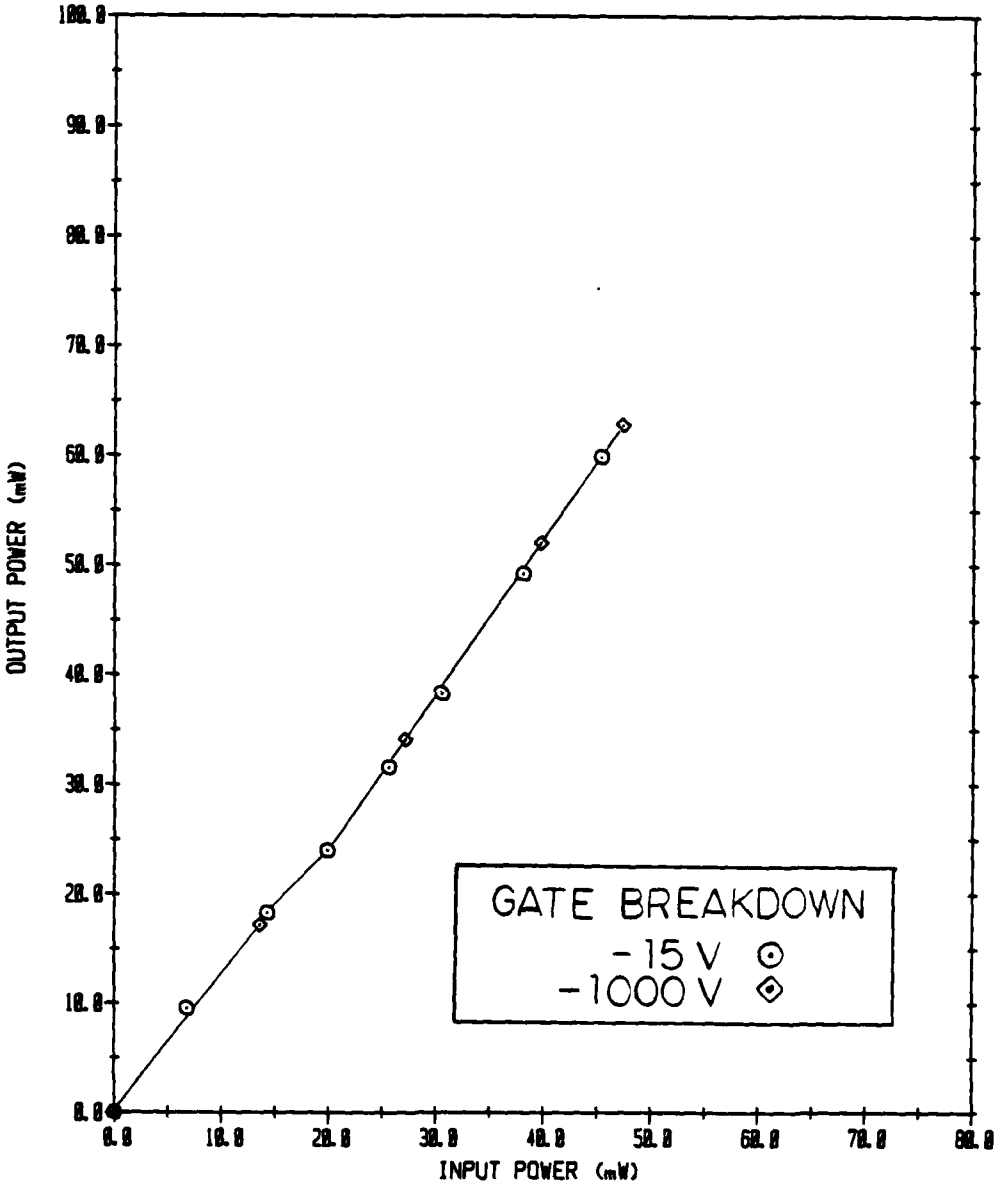

Figure 5.16. Simulated 10 GHz output power as a function of 10 GHz input power with and without reverse breakdown gate current. Drain-source bias: 7.50 V. Gate-source bias: -5.00 V.

6. CONCLUSIONS AND RECOMMENDATIONS

The purpose of this work was to improve nonlinear MESFET modeling techniques and concurrently explore large-signal circuit simulation methods in order to facilitate the design of circuits involving the large-signal operation of microwave MESFETs.

6.1 MESFET MODELING

In particular, the goal was to keep the MESFET model as close as possible to a first principle approach such as advanced by Yamaguchi and Kodera (26), and rely as little as possible on extensive additional experimental characterization which would need to be repeated for each new transistor under investigation. To this end, the Madjar-Rosenbaum (29) implementation of the Yamaguchi and Kodera model for charge transport under the gate of the transistor has been retained with the only direct modification being the inclusion of temperature effects through adjustment of the electron V(E) relation as proposed by Neidert (40).

The consequences of the neglect of a charge accumulation phenomenon in the channel in the original Yamaguchi and Kodera device simulations have been examined and found to yield acceptable results in circuit

simulations. An attempt was made to implement a charge accumulation model developed by Shur and Eastman (27) for use with the Yamaguchi and Kodera FET model, and it was found to be unsuitable. Moreover, an investigation of the theoretical foundation of the Shur and Eastman model revealed the questionable approach of applying traveling Gunn domain theory to the static charge accumulation. Negative g_D in the static I-V characteristics at low gate-source bias voltages, which is attributed by many authors to the charge accumulation phenomenon, was discovered to be adequately modeled by the MESFET model without a charge accumulation correction, if the drain current calculations were performed at temperatures corresponding to the power being dissipated in the transitor. The thermal origin of negative g_D means that it is not observed at microwave frequencies, because the thermal time constants are orders of magnitude greater than a microwave period.

Substrate and gate conduction currents are two issues not addressed by Yamaguchi and Kodera. To model these effects on an exclusively first principle basis would require a repetition of their two-dimensional device simulations. Consequently, it was decided to augment the basic MESFET model with external elements. Substrate current is handled by a linear resistance connected between the drain and source terminals. The conductance

is determined experimentally from the g_D of the transistor under test at cut-off. The gate conduction current is modeled by a pair of diodes connected between the gate-source and gate-drain terminals. The I-V characteristics for both diodes is a piecewise-linear approximation to static characteristics measured for the FET. Both measurements are simple to perform, not representing any great inconvenience. The substrate current especially tends to vary among different transistors of the same manufacturer's model, probably due to inadequately controlled conditions during processing. It is therefore easier to measure than it is to model from theory.

Parasitic reactances and resistances are also not part of the basic model. Values for the resistances are determined through the comparison of measured and calculated static I-V characteristics. There is also a significant variation for these spreading and contact resistances among transistors of the same type. The parasitic reactances depend upon the MESFET packaging. Their values are determined by calculating small-signal S-parameters using the MESFET model in a physically motivated equivalent circuit, and comparing the result with measured S-parameters. This procedure was performed manually at one bias condition, and using the resulting

reactance values, calculated and measured S-parameters were observed to agree under differing bias conditions.

Having achieved static and small-signal match-up, the next step was to investigate the large-signal effectiveness of the model by comparing circuit simulation results with acutual experiments. A single stage, common-source MESFET amplifier was constructed and operated over a range of bias voltages and input drive levels, well into the large-signal regime, while bias currents, and first and second harmonic power were measured. The experimental results at one gate bias voltage were used to determine unknown element values in the model circuit. Afterward, simulated results agreed closely with experimental results for all bias voltages. The effect of reverse gate breakdown current on gain saturation was examined by conducting simulations with and without such current and found to be negligible.

The extended MESFET model has been demonstrated to be useful for static, small-signal, and large-signal applications. The kernel remains first principle, and therefore could be used to model transistors before they are produced, for device optimization. The supplementary characterization measurements are, in part, the price paid for the simplicity and economy of the model. For the present state of reproducibility in MESFET manufacture, the trade-off is a profitable one. This lack of

uniformity in transistors is also a stumbling block for the use of such a MESFET model in routine computer aided circuit design applications. However, the MESFET model is presently useful for gaining device and large-signal circuit design insights.

6.2 LARGE-SIGNAL CIRCUIT SIMULATION METHODS

The ultimate value of any dynamic, nonlinear device model hinges upon the large-signal circuit analysis and design methods that utilize it. Although graphical or numerical root solving techniques are useful for obtaining static, nonlinear circuit solutions such as I-V characteristics, they are not adequate for obtaining large-signal responses because of the presence of reactive elements.

The conventional method (70) for obtaining large-signal results is the time-domain numerical integration of the state variable equations describing the transistor and circuit, as demonstrated in Chapter 3.. The size of the system of ordinary differential equations which is integrated increases with the number of reactive elements in the circuit, both linear and nonlinear. Most of the elements in a microwave transistor circuit are linear, and the resulting sytem of equations can be large. There were eight state variable equations for the simple

frequency doubler circuit in Chapter 3. Another difficulty arises from the presence of distributed components, which must be represented with lumped element approximations.

Time-domain numerical integration is an ideal method for obtaining transient responses. However, if a steady-state response is sought, it may be necessary to integrate over tens or hundreds of microwave periods for the transient response to die out - depending on the range of time constants associated with the circuit. The dissimilar time constant problem is particularly troublesome in handling D. C. bias circuits.

The result of time-domain simulation is a set of waveforms for the state variables. These must be further processed through a discrete Fourier transform to obtain frequency-domain information of interest to the experimenter or designer. The waveforms can be fairly detailed, depending on the time step size used in the numerical integration. The significance of the detail must be evaluated, keeping in mind the frequency limitations of the transistor and circuit modeling.

The disadvantages of numerical integration for steady-state simulation motivated the creation of the large-signal, frequency-domain simulation technique which was described in Chapter 4 and demonstrated in Chapter 5. The circuit is partitioned into linear and nonlinear

subnetworks. The linear network is characterized in the frequency-domain by a hybrid matrix relating phasor voltages and currents. There are no problems in handling large linear networks or distributed linear components, as long as the frequency response can be calculated or measured. The steady-state currents and voltages are represented as as sums of harmonically related sinusoids. Solutions are obtained by matching the phasor currents for each frequency component at the linear-nonlinear interface using a nonlinear optimization algorithm.

A potential pitfall was the efficient determination of the frequency-domain response of the nonlinear subnetwork (in this case the MESFET model). Previous authors (35) have used time-domain numerical integration for this purpose, followed by a discrete Fourier transform. This is the same as the standard integration simulation approach, but performed only for the nonlinear subnetwork. The need for this time consuming procedure has been eliminated by modifying the nonlinear MESFET model so that the instantaneous values of the terminal currents are explicit functions of the instantaneous values of the terminal voltages, and their derivatives with respect to time. Additionally, the nonlinear circuit response is calculated only for the minimum number of sample times for one microwave period as required by the discrete Fourier transform (and the Nyquist sampling

theorem). Compared with the numerical integration approach using DIFSUB (65), the nonlinear subnetwork response computation time is reduced by more than two orders of magnitude.

The frequency-domain approach is clearly preferable over the conventional time-domain integration simulation method for the steady-state analysis of microwave circuits in which the frequency components of the currents and voltages are harmonically related.

6.3 APPLICATIONS

Small-signal transistor models and linear circuit analysis are useful for amplifier design, but quickly becomes inadequate at higher power levels or for applications where performance is sensitive to nonlinear distortion. Also, mixer and self-limiting oscillator circuits depend on the transistor's nonlinearities for their operation.

6.3.1 Amplifiers and Mixers

Harmonic distortion and gain saturation for MESFET amplifiers have been investigated in Chapter 5 using a frequency-domain simulation technique to obtain steady-state circuit response. There are other nonlinear

aspects of amplifier performance that are also important: (i.) intermodulation distortion - the production of undesireable signal components in the passband of the amplifier from two or more desired signal components; (ii.) cross modulation - the transfer of modulation from one signal component to another; and (iii.) amplitude modulation to phase modulation conversion due to reactive nonlinearities. For mixer applications an intermodulation signal component is desired.

These additional aspects of nonlinear performance differ from gain saturation and harmonic distortion in that they usually involve closely spaced frequency components which are not harmonically related. This presents a problem for circuit simulation using a classical numerical integration approach because the modulation and beat frequencies are typically orders of magnitude smaller than the microwave carrier frequencies, necessitating integration over hundreds or thousands of microwave periods after steady-state has been achieved. This is prohibitively expensive. The only exception would be the special case in which the signal components are harmonically related, which might be desired for some mixers (71).

A technique that is often used for mixers is the approximation of the nonlinearities by truncated Taylor series which are used to directly calculate frequency

components. This is valid only for frequency independent (i.e. purely resistive) circuits, and is of limited value to the microwave circuit designer. A related method that has been applied to microwave mixers and amplifiers (72,73) is the use of a Taylor series approximation in a Volterra series analysis, which is a nonlinear generalization (74) of the familiar convolution integral. The drawbacks of the Volterra series approach are: (i.) the nonlinear element characteristics must be approximated by a power series, and more importantly, (ii.) the Volterra integral becomes intractable except for mild nonlinearities.

The limitations of these conventional methods motivates the examination of the frequency-domain simulation algorithm which was developed in Chapter 4 for harmonic distortion analysis, to see if it can be adapted to handle closely spaced, nonharmonically related frequency components. The straightforward approach to calculate the frequency-domain response of the nonlinear model would be to sample the interface currents for each microwave period, corresponding to the Nyquist rate for the highest significant harmonic as was done in Chapter 4, repeating this procedure over enough microwave periods to cover a modulation or beat frequency period. This could result in the need to calculate thousands of samples for

each nonlinear optimization algorithm iteration, which is an unattractive prospect.

A more economical alternative invokes the nonbaseband version of the Nyquist sampling theorem (75) in which the microwave currents are sampled as if they had already been converted down to baseband. This involves calculating a reasonable number of interface current samples at intervals which are much greater than a microwave period, and is valid if the spectral components in the vicinities of the higher harmonics of the microwave carrier are negligible. This is equivalent to first converting the microwave frequencies to baseband, and then sampling. The baseband current samples are then processed through a discrete Fourier transform, and the resulting baseband frequency components restored to the actual microwave frequencies by shifting the frequencies upward by an amount equal to the original downconversion resulting from the sampling. Such a large-signal, frequency-domain simulation algorithm could offer a tremendous reduction in computation time when compared with the numerical integration approach, without the limitations associated with a Volterra series analysis. This is in addition to retaining the ability to use frequency-domain characterizations of the linear subnetworks, and the direct derivation of steady-state

frequency components as for the harmonic distortion implementation of the frequency-domain algorithm.

6.3.2 Oscillators

MESFET oscillators have been analyzed on a small-signal basis (3) with some success in predicting operating frequency, but performance aspects such as output power, tuning hysteresis, and injection locking require nonlinear analysis. Microwave MESFET oscillator circuits are generally self-limiting (76), with the transistor being driven into gain saturation and thus generating harmonics and exhibiting nonlinear effects.

Circuit performance can be simulated using numerical integration of the state variable equations, as done in Chapter 3 for a frequency doubler. The advantages and disadvantages of this standard approach have already been discussed. A large-signal, frequency-domain simulation method similar to the one developed in Chapter 4 might also be used, but the fundamental frequency of operation would need to be added to the list of independent variables for the nonlinear optimization algorithm because the exact frequency of operation is not known in advance. In addition to increasing the expected number of optimization algorithm iterations, computation time would also be increased because of the need to recalculate the

frequency dependent coeffecients for the frequency- to time-domain interconversion at each iteration. Using either method, many circuit simulations would be required to explore oscillator circuit design because each simulation only indicates how a specific circuit performs under specific conditions.

Direct large-signal, frequency-domain microwave oscillator design methods (77-79) have been devised for circuits in which the active element can be modeled as a nonlinear one-port. The active element is represented by a describing function (38), which in this case is a signal dependent linear resistance or admittance at each frequency component of interest. Kurokawa (77) and Kenyon (78) consider only the fundamental frequency component. Foulds and Sebastian (79) also include the second harmonic. Unfortunately when considering higher harmonics, the dimensionality of the method becomes unmanagable because in general, the describing functions depend not only on the amplitude and phase of the current or voltage at their respective frequency components, but on the amplitudes and phases at all of the other frequency components as well.

A microwave transistor may be reduced to a one-port which exhibits negative resistances over a desired frequency range by imbedding it in a suitable circuit, and the transistor in its imbedding circuit may then be used

as a one-port in a Kurokawa-type analysis (80). The frequency-domain simulation technique which was developed in Chapter 4 can be used to evaluate the describing functions at specific frequencies. The need for the advance specification of an imbedding circuit which reduces the two-port MESFET to a one-port limits the usefulness of this procedure for oscillator circuit design optimization.

Other authors (81-84) have reported frequency-domain nonlinear oscillator design methods which are based on large-signal, two-port transistor characterizaions, eliminating the need for prior reduction to a one-port. At first inspection this is an attractive prospect. Although so far, such methods have only been used in attempts to maximize output power, these procedures, if valid, could be extended to analyze tuning hysteresis, noise and injection locking performance in a manner similar to that originated by Kurokawa (77) for one-port nonlinearities. The method used for the frequency-domain characterization of the basic nonlinear MESFET model which was described in Section 4.2, might be used to calculate the required large-signal impedance or admittance matrices. This is a noniterative procedure, and the cost would be trivial.

Closer examination raises some questions about the validity of large-signal matrix characterizations for nonlinear two-ports. In common usage (37), describing

functions characterize nonlinearities with only one input signal (equivalent to a one-port in this context), although this signal may be the sum of many components. A two-port may be viewed as having two input signals (voltages, for example), and two output signals (currents, for example). The ability to relate these separate input and output signals with an (admittance) matrix composed of describing function elements requires additional investigation, which will be discussed in the next section.

6.4 LARGE-SIGNAL, TWO-PORT CHARACTERIZATIONS OF MESFETS

There have been reports (82-86) on the use of large-signal S-parameter characterizations for nonlinear two-ports, transistors in particular, for microwave circuit analysis and design. It is therefore worthwile to examine the assumptions inherent in the extension of the linear circuit S-parameter concept, and the consider the circumstances under which it is meaningful. With obvious modifications, the following discussion also applies to large-signal impedance or admittance matrix representations (81,87) for nonlinear two-ports.

For a linear two-port, reflected voltage waves, V_1^- and V_2^-, can be related to incident voltage waves, V_1^+ and V_2^+, by a S-parameter matrix at each frequency of

interest:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11}(\omega) & S_{12}(\omega) \\ S_{21}(\omega) & S_{22}(\omega) \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \qquad (6\text{-}1)$$

This formulation implies the linear superposition of V_1^+ and V_2^+. Moreover, the $S_{i,j}(\omega)$s are not, in general, uniquely defined by arbitrary values of V_1^+, V_2^+, V_1^- and V_2^-. This is because equation (6-1) represents only two equations from which the four unknown matrix elements must be determined. Ordinarily, the matrix elements are defined from additionally constrained cases which are obtained by alternately setting V_1^+ and V_2^+ to zero:

$$S_{i,j}(\omega) = \left.\frac{V_i^-}{V_j^+}\right|_{V_K^+=0,\ K\neq j} \qquad (6\text{-}2)$$

This procedure presents no difficulty with linear two-ports because the $S_{i,j}(\omega)$s are not functions of V_1^+ or V_2^+.

For nonlinear two-ports under large-signal conditions, incident and reflected voltage waves need not have a simple sinusoidal time dependence, but may be represented by sums of harmonically related sinusoids.

The ratios of the complex Fourier coefficients of these voltage waves can be taken for each frequency component to derive large-signal scattering parameters. These are also known as describing functions (38). For the sake of this discussion, the higher harmonics will be neglected and only the fundamental considered, as is customary (82-86).

In general, large-signal S-parameters are functions of the magnitudes and relative phase of both V_1^+ and V_2^+, and therefore must be determined by applying specific values of these voltage wave phasors. As indicated previously, this is not generally possible because equation (6-1) is not adequately constrained. For the general nonlinear two-port, the signal dependence precludes the possibility of alternately setting V_1^+ and V_2^+ to zero, as was done in equation (6-2) for the definition of linear two-port S-parameters. Consequently, it is easily verified that a large-signal S-parameter matrix for a nonlinear two-port can be defined from measured or simulated voltage waves only if each row of the matrix satisfies at least one of the following conditions:

1.) An element in the row is a constant.

2.) The element in the first column is a function of V_1^+ and is not a function of V_2^+.

3.) The element in the second column is a function of V_2^+ and is not a function of V_1^+.

Before using large-signal S-parameters for circuit applications, it is important to investigate whether or not they are unambiguously defined for the nonlinear two-port and measurement procedure in question. Reported large-signal, common source S-parameter measurements for power GaAs MESFETs do not clearly satisfy the above criteria. Although S_{12} might be approximated as a constant, permitting the determination of the first row elements, S_{21} and S_{22} are both functions of V_1^+. Until the sensitivities of S_{21} and S_{22} to V_2^+ have been established, the possibility exists that large-signal S-parameter characterizations could be fundamentally inappropriate for MESFETs, and should be used with caution in this context.

The problem of the lack of unique definition is separate from the commonly cited (81,86) drawbacks associated with the application of large-signal S-parameter techniques: neglect of harmonics, and the use of terminating impedances in the course of the measurements that are different from those present in actual circuit applications.

The preceeding discussion involved large-signal S-parameters, but analogous criteria must be satisfied by large-signal admittance or impedance matrices if they are to be obtained directly from measured or simulated currents and voltages. If it is possible to define one of

these three types of matrices, it is then possible to obtain the other two from the first using standard transformations (88), although they might not be directly determinable from the voltage, current, or voltage wave information. It is difficult to directly measure impedances or admittances for microwave MESFETs. The MESFET model and frequency-domain simulation algorithm presented in this report can be used to investigate the validity of large-signal two-port admittance, impedance and (indirectly) S-parameter characterizations for MESFETs in order to determine the desirability of pursuing compatible circuit design procedures. This investigation would involve conducting simulations such as reported in Chapter 5, but with signal generators at both the drain-source and gate-source ports of the transistor. It would also be worthwhile to investigate common gate and common drain configurations.

7. ACKNOWLEDGEMENT

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8. APPENDICES

APPENDIX 8.1

The Shur and Eastman Static Domain Model

The Shur and Eastman "static Gunn domain" correction (27) to the Yamaguchi and Kodera FET model (26) is used as a controlled voltage source, representing the voltage drop across the "static Gunn domain", which is inserted in series with the FET channel conductance at the drain side. This effectively reduces the drain-source voltage, and thereby the drain current, of the Yamaguchi and Kodera model when a "static domain" is present. The schematic for the drain mesh of the circuit used for common-source static drain current calculations is shown in Figure 8.1. The Shur and Eastman "static Gunn domain" voltage drop model (equation 23 in reference 27) can be written:

$$V_{DOM}(V_{DS}) = \frac{\beta}{(E_{out}-\gamma)^2}$$

where β and γ are constants, and EOUT is the magnitude of the electric field at the drain side of the gate in the Yamaguchi and Kodera model. For the present discussion, EOUT can be assumed to be proportional to VDS:

$$E_{out} \cong \alpha V_{DS}$$

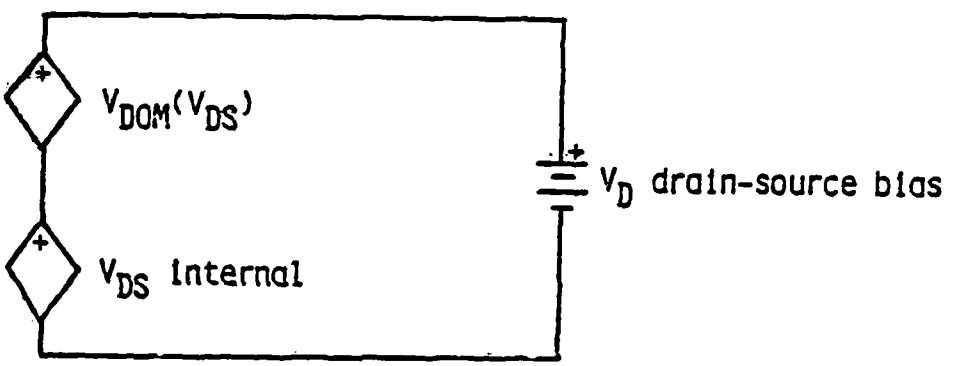

Figure 8.1. Drain mesh used for common-source static I-V calculations with the Shur and Eastman modification of the Yamaguchi and Kodera MESFET model.

resulting in:

$$V_{DOM}(V_{DS}) = \frac{\beta}{(\alpha V_{DS}-\gamma)^2}$$

Using Kirchoff's voltage law for the mesh, we have:

$$V_D = V_{DOM} + V_{DS}$$

$$= \frac{\beta}{(\alpha V_{DS}-\gamma)^2} + V_{DS}$$

which may be regarded as the simultaneous solution of:

$$f_1(V_{DS}) = V_{DS}$$

and

$$f_2(V_{DS}) = V_D - \frac{\beta}{(\alpha V_{DS}-\gamma)^2}$$

igure 8.2 is a graphical presentation of this problem. The desired roots are the ones at lowest VDS. There is no solution for values of V_D less than V_{D2}, indicating no "static Gunn domain" formation, in which case VDS = VD. As soon as $V_D = V_{D2}$ is achieved, V_{DS} is immediately reduced to the value indicated by point A . This demonstrates the inherent drain current discontinuity in

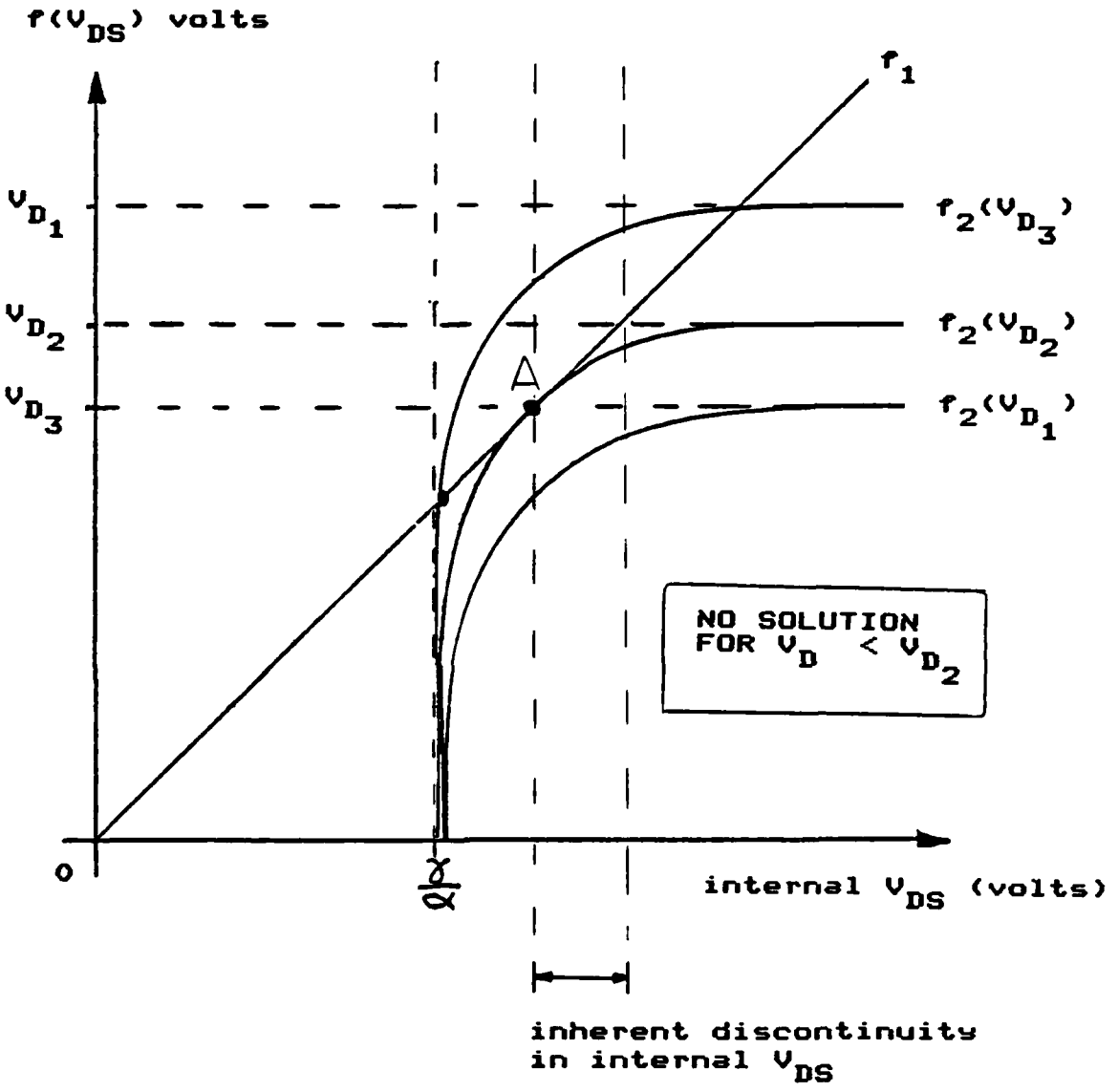

Figure 8.2. Approximate graphical solution for common-source I-V characterstics using the Shur and Eastman modification to the Yamaguchi and Kodera MESFET model.

the Shur and Eastman model which is not observed experimentally.

APPENDIX 8.2

The Impedance of a Capacitance Measured Through a Time Delay in Voltage

Assuming sinusoidal excitation, the voltage across and the current through a capacitance can be expressed:

$$v(t) = Re\{Ve^{j\omega t}\}$$

$$i(t) = Re\{Ie^{j\omega t}\}$$

The voltage, delayed by a time, τ is:

$$v(t-\tau) = Re\{(Ve^{-j\omega\tau})e^{j\omega t}\}$$

The impedance of the capacitance is:

$$Z_C = \frac{V_C}{I_C} = \frac{1}{j\omega C}$$

If the impedance is measured through the τ second time delay as indicated in Figure 8.3, it becomes:

$$Z_{IN} = \frac{1}{\omega C}\,[\sin(\omega\tau) - j\cdot\cos(\omega\tau)]$$

The effect of the time delay is to add a real part to the otherwise purely imaginary impedance of the reactive element.

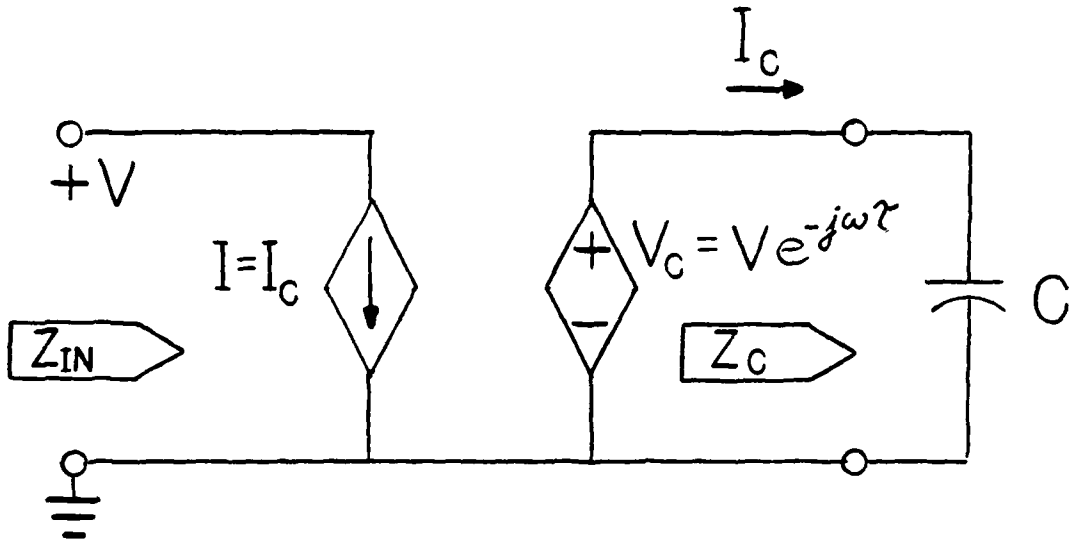

Figure 8.3. Circuit diagram using controlled current and voltage sources to measure the impedance of a capacitance through a time delay in the voltage.

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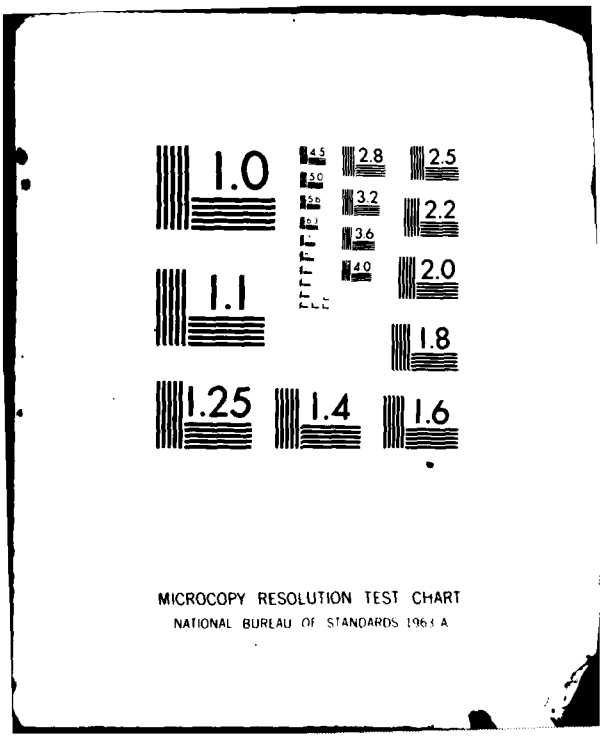
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